PXI Express™

NI PXIe-1085 Series User Manual

Vertrieb durch AMC

AMC – Analytik & Messtechnik GmbH Chemnitz

Heinrich-Lorenz-Str. 55 Tel.: +49/371/38388-0
09120 Chemnitz Fax: +49/371/38388-99
E-Mail: info@amc-systeme.de Web: www.amc-systeme.de

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About This Manual

The *NI PXIe-1085 Series User Manual* describes the features of the NI PXIe-1085 Series chassis and contains information about configuring the chassis, installing the modules, and operating the chassis.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- IEEE 1101.1-1991, *IEEE Standard for Mechanical Core Specifications for Microcomputers Using IEC 603-2 Connectors*
- IEEE 1101.10, *IEEE Standard for Additional Mechanical Specifications for Microcomputers Using IEEE 1101.1 Equipment Practice*
- *PICMG EXP.0 R1.0 CompactPCI Express Specification*, PCI Industrial Computers Manufacturers Group
- *PCI Express Base Specification*, Revision 1.1, PCI Special Interest Group
- *PXI-5 PXI Express Hardware Specification*, Revision 2.0, PXI Systems Alliance

1

Getting Started

This chapter describes the key features of the NI PXIe-1085 Series chassis and lists the kit contents and optional equipment you can order from National Instruments.

Unpacking

Carefully inspect the shipping container and the chassis for damage. Check for visible damage to the metal work. Check to make sure all handles, hardware, and switches are undamaged. Inspect the inner chassis for any possible damage, debris, or detached components. If damage appears to have been caused during shipment, file a claim with the carrier. Retain the packing material for possible inspection and/or reshipment.

What You Need to Get Started

The NI PXIe-1085 Series chassis kit contains the following items:

- ☐ NI PXIe-1085 12 GB/s chassis or NI PXIe-1085 24 GB/s chassis
- ☐ Filler panels
- ☐ AC power cable—refer to Table 1-1 for AC power cables
- ☐ *NI PXIe-1085 Series User Manual*
- ☐ Software media with *PXI Platform Services 3.0* or higher
- ☐ Chassis number labels
- ☐ Screw to permanently restrain the front panel
- ☐ Eight-position connector for remote voltage monitoring and control

Table 1-1. AC Power Cables

Power Cable	Reference Standards
Standard 120 V (USA)	ANSI C73.11/NEMA 5-15-P/IEC83
Switzerland 220 V	SEV
Australia 240 V	AS C112
Universal Euro 230 V	CEE (7), II, IV, VII IEC83
United Kingdom 230 V	BS 1363/IEC83

If you are missing any of the items listed in Table 1-1, or if you have the incorrect AC power cable, contact National Instruments.

Key Features

The NI PXIe-1085 Series chassis combines a high-performance 18-slot PXI Express backplane with a high-output power supply and a structural design that has been optimized for maximum usability in a wide range of applications. The chassis' modular design ensures a high level of maintainability, resulting in a very low mean time to repair (MTTR). The NI PXIe-1085 Series chassis fully complies with the *PXI-5 PXI Express Hardware Specification*, offering advanced timing and synchronization features.

The key features of the NI PXIe-1085 Series chassis include the following:

High Performance for Instrumentation Requirements

- **NI PXIe-1085 12 GB/s chassis**—Up to 4 GB/s (single direction) per PXI Express slot dedicated bandwidth (x8 Gen-2 PCI Express).
- **NI PXIe-1085 24 GB/s chassis**—Up to 8 GB/s (single direction) per PXI Express slot dedicated bandwidth (x8 Gen-3 PCI Express).
- 38.25 W per slot cooling meets increased PXI Express cooling requirements
- Low-jitter internal 10 MHz reference clock for PXI/PXI Express slots with ± 25 ppm stability
- Low-jitter internal 100 MHz reference clock for PXI Express slots with ± 25 ppm stability
- Quiet operation for 0 to 30 °C at 51.2 dBA
- Variable speed fan controller optimizes cooling and acoustic emissions
- Remote power-inhibit control
- Complies with PXI and CompactPCI Specifications

High Reliability

- 0 to 55 °C extended temperature range
- Power supply, temperature, and fan monitoring
- Field replaceable power supply and fans

Multi-Chassis Support

- PXI Express System Timing Slot for tight synchronization across chassis
- Front panel CLK10 I/O connectors
- Switchless CLK10 routing

Optional Features

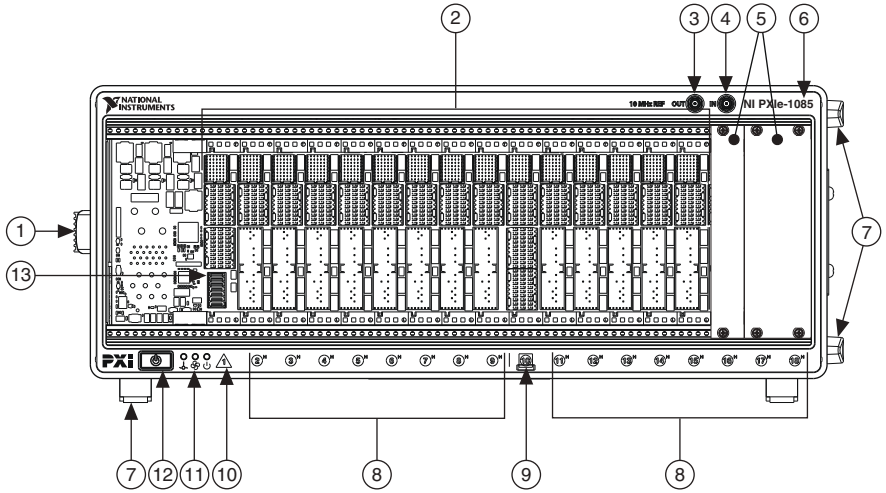
- Front and rear rack-mount kits
- Replacement power supply
- EMC filler panels
- Slot blockers for improved cooling performance
- Factory installation services
- Replacement fan modules

Chassis Description

Figures 1-1 and 1-2 show the key features of the NI PXIe-1085 Series chassis front and back panels. Figure 1-1 shows the front view of the series chassis. Figure 1-2 shows the rear view of the series chassis.

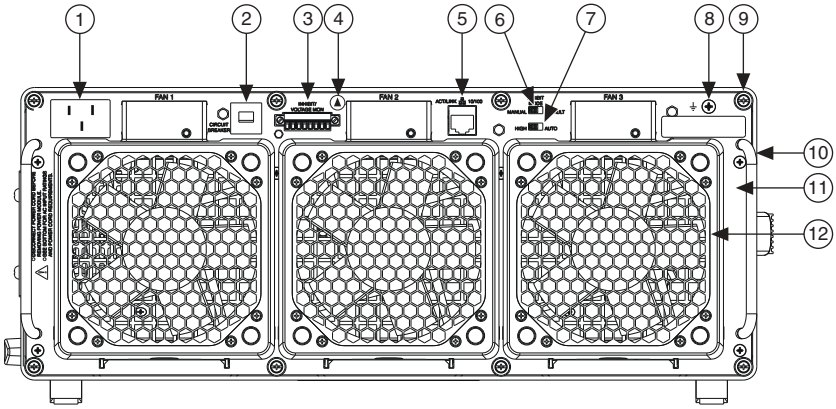
Note The NI PXIe-1085 24 GB/s chassis can be identified by the blue **24 GB/s** graphic to the left of the 10 MHz REF OUT SMA connector. The NI PXIe-1085 12 GB/s chassis does not have this mark.

Figure 1-1. Front View of the NI PXIe-1085 Series Chassis



1	Chassis Carry Handle	8	PXI Express Hybrid Peripheral Slots (16x)
2	Backplane Connectors	9	PXI Express System Timing Slot
3	10 MHz REF OUT SMA	10	PXI Express System Controller Slot
4	10 MHz REF IN SMA	11	Temperature, Fan, and Power LEDs
5	PXI Filler Panels	12	Power Inhibit Switch
6	Chassis Model Name	13	System Controller Expansion Slot
7	Removable Feet		

Figure 1-2. Rear View of the NI PXIe-1085 Series Chassis



1	Universal AC Input	7	Fan Speed Selector Switch
2	Push-Reset Circuit Breaker	8	Chassis Ground Screw
3	Remote Inhibit and Voltage Monitoring Connector	9	Power Supply Shuttle Mounting Screws (8x)
4	Electrostatic-Sensitive Device Symbol	10	Power Supply Shuttle Handle (2x)
5	Ethernet Port	11	Power Supply Shuttle
6	Inhibit Mode Selector Switch	12	Fan Module (3x)

Optional Equipment

Contact National Instruments to order the following options for the NI PXIe-1085 Series chassis.

EMC Filler Panels

Optional EMC filler panel kits are available from National Instruments.

Rack Mount Kit

There are two required kits for mounting the NI PXIe-1085 Series chassis into a rack. The first is a pair of mounting brackets for use on the front of the chassis. The second is a rear rack mount kit. For more information, refer to Figure A-3, *NI Chassis Rack Mount Kit Components*.

Slot Blockers

Optional PXI Slot Blocker kits are available from National Instruments for improved thermal performance when all slots are not used.

Replacement Power Supply

Optional replacement power supply kits are available from National Instruments. You easily can install replacement power supplies without the use of tools.

Replacement Fan Modules

Optional replacement fan modules are available from National Instruments. You easily can install fans in seconds without the use of tools and without powering down the system.

NI PXIe-1085 Series Backplane Overview

This section provides an overview of the backplane features for the NI PXIe-1085 Series chassis.

Note The differences between the NI PXIe-1085 12 GB/s chassis and the NI PXIe-1085 24 GB/s chassis are noted where applicable.

Interoperability with CompactPCI

The design of the NI PXIe-1085 Series chassis provides you the flexibility to use the following devices in a single PXI Express chassis:

- PXI Express compatible products
- CompactPCI Express compatible 2-Link system controller products
- CompactPCI Express compatible Type-2 peripheral products
- PXI peripheral products modified to fit in a hybrid slot
- Standard CompactPCI peripheral products modified to fit in a hybrid slot

System Controller Slot

NI PXIe-1085 12 GB/s

The system controller slot is Slot 1 of the chassis and is a 2-Link configuration system slot as defined by the CompactPCI Express and PXI Express specifications. It has three system controller expansion slots for system controller modules that are wider than one slot. These slots allow the system controller to expand to the left to prevent the system controller from using peripheral slots.

The backplane connects the system slot to two PCI Express switches using a Gen-2 x8 and a Gen-2 x16 PCI Express link. These switches distribute PCI Express connections to the peripheral slots and to two PCI Express-to-PCI bridges to provide PCI buses to the hybrid peripheral slots. Refer to Figure 1-3 for an overview of the NI PXIe-1085 Series architecture.

System slot link 1 is a Gen-2 x8 PCI Express link to PCI Express switch 1, providing a nominal bandwidth of 4 GB/s (single direction) between the system controller and PCI Express switch 1. PXI Express peripheral slots 2-10 are connected to PCI Express switch 1 with Gen-2 x8 PCI Express links and are downstream of system slot link 1. PCI Express-to-PCI bridge 1 is connected to PCI Express switch 1 and provides a 32-bit, 33 MHz PCI bus for hybrid peripheral slots 2-9.

System slot link 2 is a Gen-2 x16 PCI Express link to PCI Express switch 2, providing a nominal bandwidth of 8 GB/s (single direction) between the system controller slot and PCI Express switch 2. PXI Express peripheral slots 11-18 are connected to PCI Express switch 2 with Gen-2 x8 PCI Express links and are downstream of system slot link 2. PCI Express-to-PCI bridge 2 is connected to PCI Express switch 2 and provides a 32-bit, 33 MHz PCI bus for hybrid peripheral slots 11-18.

The system controller slot also has connectivity to some PXI features such as: PXI_CLK10, PXI Star, PXI Trigger Bus and PXI Local Bus 6.

By default, the system controller will control the power supply with the PS_ON# signals. A logic low on this line will turn the power supply on.

Note The Inhibit Mode switch on the rear of the chassis must be in the **Default** position for the system controller to have control of the power supply. Refer to the *Inhibit Mode Switch* section of Chapter 2, *Installation and Configuration*, for details about the Inhibit Mode switch.

NI PXIe-1085 24 GB/s

The system controller slot is Slot 1 of the chassis and is a 2-Link configuration system slot as defined by the CompactPCI Express and PXI Express specifications. It has three system controller expansion slots for system controller modules that are wider than one slot. These slots allow the system controller to expand to the left to prevent the system controller from using peripheral slots.

The backplane connects the system slot to two PCI Express switches using a Gen-3 x8 and a Gen-3 x16 PCI Express link. These switches distribute PCI Express connections to the peripheral slots and to two PCI Express-to-PCI bridges to provide PCI buses to the hybrid peripheral slots. Refer to Figure 1-3 for an overview of the NI PXIe-1085 Series architecture.

System slot link 1 is a Gen-3 x8 PCI Express link to PCI Express switch 1, providing a nominal bandwidth of 8 GB/s (single direction) between the system controller and PCI Express switch 1. PXI Express peripheral slots 2-10 are connected to PCI Express switch 1 with Gen-3 x8 PCI Express links and are downstream of system slot link 1. PCI Express-to-PCI bridge 1 is connected to PCI Express switch 1 and provides a 32-bit, 33 MHz PCI bus for hybrid peripheral slots 2-9. PCI Express switch 1 also is connected to PCI Express switch 2 with a Gen-3 x8 PCI Express link for advanced backplane configurations.

System slot link 2 is a Gen-3 x16 PCI Express link to PCI Express switch 2, providing a nominal bandwidth of 16 GB/s (single direction) between the system controller slot and PCI Express switch 2. PXI Express peripheral slots 11-18 are connected to PCI Express switch 2 with Gen-3 x8 PCI Express links and are downstream of system slot link 2. PCI Express-to-PCI bridge 2 is connected to PCI Express switch 2 and provides a 32-bit, 33 MHz PCI bus for hybrid peripheral slots 11-18. PCI Express switch 2 also is connected to PCI Express switch 1 with a Gen-3 x8 PCI Express link for advanced backplane configurations.

The system controller slot also has connectivity to some PXI features such as: PXI_CLK10, PXI Star, PXI Trigger Bus and PXI Local Bus 6.

By default, the system controller will control the power supply with the PS_ON# signals. A logic low on this line will turn the power supply on.

Note The Inhibit Mode switch on the rear of the chassis must be in the Default position for the system controller to have control of the power supply. Refer to the *Inhibit Mode Switch* section of Chapter 2, *Installation and Configuration*, for details about the Inhibit Mode switch.

Hybrid Peripheral Slots

The chassis provides 16 hybrid peripheral slots as defined by the *PXI-5 PXI Express Hardware Specification*: slots 2-9 and slots 11-18. A hybrid peripheral slot can accept the following peripheral modules:

- **NI PXIe-1085 12 GB/s**—A PXI Express peripheral with x8, x4, or x1 PCI Express link through a switch to the system slot. Each PXI Express peripheral slot can link up to a Gen-2 x8 PCI Express, providing a maximum nominal single-direction bandwidth of 4 GB/s.
- **NI PXIe-1085 24 GB/s**—A PXI Express peripheral with x8, x4, or x1 PCI Express link through a switch to the system slot. Each PXI Express peripheral slot can link up to a Gen-3 x8 PCI Express, providing a maximum nominal single-direction bandwidth of 8 GB/s.
- A CompactPCI Express Type-2 Peripheral with x8, x4, or x1 PCI Express link through a switch to the system slot.
- A hybrid-compatible PXI Peripheral module that has been modified by replacing the J2 connector with an XJ4 connector installed in the upper eight rows of J2. Refer to the *PXI Express Specification* for details. The PXI Peripheral communicates through the backplane's 32-bit PCI bus.
- A CompactPCI 32-bit peripheral on the backplane's 32-bit PCI bus.

The hybrid peripheral slots provide full PXI Express functionality and 32-bit PXI functionality except for PXI Local Bus. The hybrid peripheral slot only connects to PXI Local Bus 6 left and right.

Figure 1-3. NI PXIe-1085 12 GB/s PCI Express Backplane Diagram

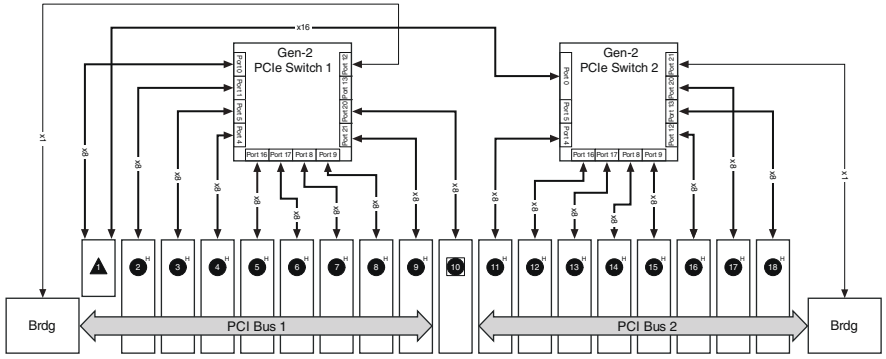
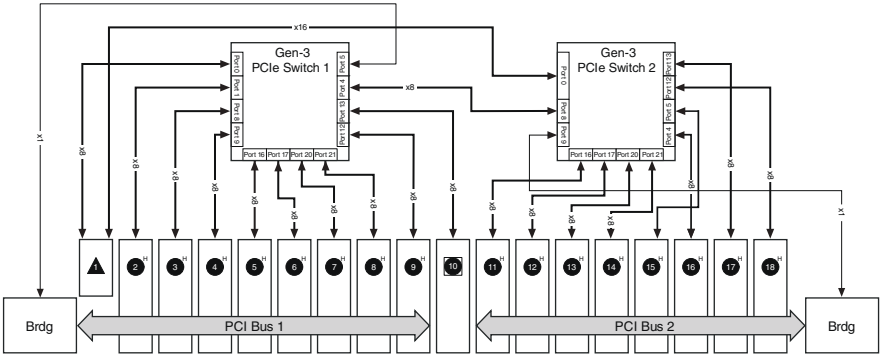


Figure 1-4. NI PXIe-1085 24 GB/s PCI Express Backplane Diagram



System Timing Slot

The System Timing Slot is slot 10. The system timing slot will accept the following peripheral modules:

- **NI PXIe-1085 12 GB/s**—A PXI Express System Timing Module with x8, x4, or x1 PCI Express link to the system slot through a PCI Express switch. Each PXI Express peripheral slot can link up to a Gen-2 x8 PCI Express, providing a maximum nominal single-direction bandwidth of 4 GB/s.
- **NI PXIe-1085 24 GB/s**—A PXI Express System Timing Module with x8, x4, or x1 PCI Express link to the system slot through a PCI Express switch. Each PXI Express peripheral slot can link up to a Gen-3 x8 PCI Express, providing a maximum nominal single-direction bandwidth of 8 GB/s.
- A PXI Express Peripheral with x8, x4, or x1 PCI Express link to the system slot through a PCI Express switch.
- A CompactPCI Express Type-2 Peripheral with x8, x4, or x1 PCI Express link to the system slot through a PCI Express switch.

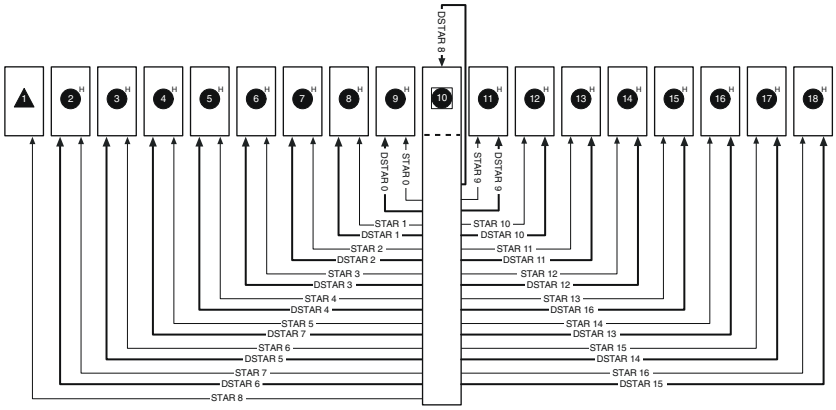
The system timing slot has 3 dedicated differential pairs (PXIe_DSTAR) connected from the TP1 and TP2 connectors to the XP3 connector for each PXI Express hybrid peripheral slot, as well as routed back to the XP3 connector of the system timing slot as shown in Figure 1-5. The PXIe_DSTAR pairs can be used for high-speed triggering, synchronization and clocking. Refer to the *PXI Express Specification* for details.

The system timing slot also has a single-ended (PXI Star) trigger connected to every slot. Refer to Figure 1-5 for details.

The system timing slot has a pin (PXI_CLK10_IN) through which a system timing module may source a 10 MHz clock to which the backplane will phase-lock. Refer to the *System Reference Clock* section for details.

The system timing slot has a pin (PXIe_SYNC_CTRL) through which a system timing module can control the PXIe_SYNC100 timing. Refer to the *PXI Express Specification* and the *PXIe_SYNC_CTRL* section of this chapter for details.

Figure 1-5. PXI Express Star Connectivity Diagram



PXI Local Bus

The PXI backplane local bus is a daisy-chained bus that connects each peripheral slot with adjacent peripheral slots to the left and right, as shown in Figure 1-6.

The backplane routes PXI Local Bus 6 between all slots. The left local bus 6 from slot 1 is not routed anywhere and the right local bus signals from slot 18 are not routed anywhere.

Local bus signals may range from high-speed TTL signals to analog signals as high as 42 V.

Initialization software uses the configuration information specific to each adjacent peripheral module to evaluate local bus compatibility.

PXI Trigger Bus

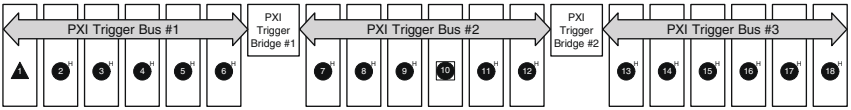
All slots on the same PXI bus segment share eight PXI trigger lines. You can use these trigger lines in a variety of ways. For example, you can use triggers to synchronize the operation of several different PXI peripheral modules. In other applications, one module located in the system timing slot can control carefully timed sequences of operations performed on other modules in the system. Modules can pass triggers to one another, allowing precisely timed responses to asynchronous external events the system is monitoring or controlling.

The PXI trigger lines from adjacent PXI trigger bus segments can be routed in either direction across the PXI trigger bridges through buffers. This allows you to send trigger signals to, and receive trigger signals from, every slot in the chassis. Static trigger routing (user-specified line and directional assignments) can be configured through Measurement & Automation Explorer

(MAX). Dynamic routing of triggers (automatic line assignments) is supported through certain National Instruments drivers like NI-DAQmx.

Note Although any trigger line may be routed in either direction, it cannot be routed in more than one direction at a time.

Figure 1-6. PXI Trigger Bus Connectivity Diagram



System Reference Clock

The NI PXIe-1085 Series chassis supplies PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 independently driven to each peripheral slot.

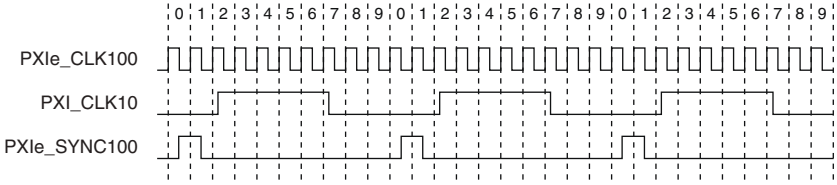
An independent buffer (having a source impedance matched to the backplane and a skew of less than 1 ns between slots) drives PXI_CLK10 to each slot. You can use this common reference clock signal to synchronize multiple modules in a measurement or control system.

An independent buffer drives PXIe_CLK100 to each peripheral slot. These clocks are matched in skew to less than 100 ps. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_CLK100 so that when there is no peripheral or a peripheral that does not connect to PXIe_CLK100, there is no clock being driven on the pair to that slot.

An independent buffer drives PXIe_SYNC100 to each peripheral slot. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_SYNC100 so that when there is no peripheral or a peripheral that does not connect to PXIe_SYNC100, there is no SYNC100 signal being driven on the pair to that slot.

PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 have the default timing relationship described in Figure 1-7.

Figure 1-7. System Reference Clock Default Behavior



To synchronize the system to an external clock, you can drive PXI_CLK10 from an external source through the PXI_CLK10_IN pin on the System Timing Slot. Refer to Table B-8, *XP4 Connector Pinout for the System Timing Slot*, for the pinout. When a 10MHz clock is detected

on this pin, the backplane automatically phase-locks the PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 signals to this external clock and distributes these signals to the slots. Refer to Appendix A, *Specifications*, for the specification information for an external clock provided on the PXI_CLK10_IN pin of the system timing slot.

You also can drive a 10 MHz clock on the 10 MHz REF IN connector on the front panel of the chassis. When a 10 MHz clock is detected on this connector, the backplane automatically phase-locks the PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 signals to this external clock and distributes these signals to the slots. Refer to Appendix A, *Specifications*, for the specification information for an external clock provided on the 10 MHz REF IN connector on the front panel of the chassis.

If the 10 MHz clock is present on both the PXI_CLK10_IN pin of the System Timing Slot and the 10 MHz REF IN connector on the front of the chassis, the signal on the System Timing Slot is selected. Refer to Table 1-2 which explains how the 10 MHz clocks are selected by the backplane.

Table 1-2. Backplane External Clock Input Truth Table

System Timing Slot PXI_CLK10_IN	Front Chassis Panel 10 MHz REF IN	Backplane PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100
No clock present	No clock present	Backplane generates its own clocks
No clock present	10 MHz clock present	PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 all phase-locked to Front Chassis Panel—10 MHz REF IN
10 MHz clock present	No clock present	PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 all phase-locked to System Timing Slot— PXI_CLK10_IN
10 MHz clock present	10 MHz clock present	PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 all phase-locked to System Timing Slot— PXI_CLK10__IN

A copy of the backplane's PXI_CLK10 is exported to the 10 MHz REF OUT connector on the front panel of the chassis. This clock is driven by an independent buffer. Refer to Appendix A, *Specifications*, for the specification information for the 10 MHz REF OUT signal on the front panel of the chassis.

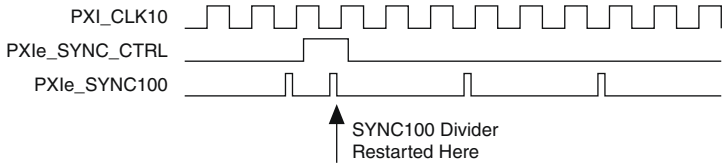
PXIe_SYNC_CTRL

PXIe_SYNC100 is by default a 10 ns pulse synchronous to PXI_CLK10. The frequency of PXIe_SYNC100 is 10/*n* MHz, where *n* is a positive integer. The default for *n* is 1, giving PXIe_SYNC100 a 100 ns period. However, the backplane allows *n* to be programmed to other integers. For instance, setting *n* = 3 gives a PXIe_SYNC100 with a 300 ns period while still maintaining its phase relationship to PXI_CLK10. The value for *n* may be set to any positive integer from 1 to 255.

The system timing slot has a control pin for PXIe_SYNC100 called PXIe_SYNC_CTRL for use when *n* > 1. Refer to Table B-7, *XP3 Connector Pinout for the System Timing Slot*, for system timing slot pinout. Refer to Appendix A, *Specifications*, for the PXIe_SYNC_CTRL input specifications.

By default, a high-level detected by the backplane on the PXIe_SYNC_CTRL pin causes a synchronous restart for the PXIe_SYNC100 signal. On the next PXI_CLK10 edge the PXIe_SYNC100 signal will restart. This will allow several chassis to have their PXIe_SYNC100 in phase with each other. Refer to Figure 1-8 for timing details with this method.

Figure 1-8. PXIe_SYNC100 at 3.33 MHz Using PXIe_SYNC_CTRL as Restart



2 Installation and Configuration

This chapter describes how to prepare and operate the NI PXIe-1085 Series chassis.

Before connecting the chassis to a power source, read this chapter and the *Read Me First: Safety and Electromagnetic Compatibility* document included with your kit.

Safety Information

Cautions Before undertaking any troubleshooting, maintenance, or exploratory procedure, carefully read the following caution notices.

Protection equipment may be impaired if equipment is not used in the manner specified.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

- **Chassis Grounding**—The chassis requires a connection from the premise wire safety ground to the chassis ground. The earth safety ground must be connected during use of this equipment to minimize shock hazards. Refer to the *Connecting Safety Ground* section for instructions on connecting safety ground.
- **Live Circuits**—Operating personnel and service personnel *must* not remove protective covers when operating or servicing the chassis. Adjustments and service to internal components must be undertaken by qualified service technicians. During service of this product, the mains connector to the premise wiring must be disconnected. Dangerous voltages may be present under certain conditions; use extreme caution.
- **Explosive Atmosphere**—Do *not* operate the chassis in conditions where flammable gases are present. Under such conditions, this equipment is unsafe and may ignite the gases or gas fumes.
- **Part Replacement**—Only service this equipment with parts that are exact replacements, both electrically and mechanically. Contact National Instruments for replacement part information. Installation of parts with those that are not direct replacements may cause harm to personnel operating the chassis. Furthermore, damage or fire may occur if replacement parts are unsuitable.
- **Modification**—Do *not* modify any part of the chassis from its original condition. Unsuitable modifications may result in safety hazards.

Chassis Cooling Considerations

The NI PXIe-1085 Series chassis is designed to operate on a bench or in an instrument rack. The chassis must be oriented horizontally for benchtop use. Vertical orientation with the chassis handle up is not a supported configuration. Regardless of the configuration, you must provide the cooling clearances as outlined in the following sections.

Providing Adequate Clearance

The primary cooling exhaust vent for the NI PXIe-1085 Series is on the top of the chassis. The primary intake vent is on the rear of the chassis. The secondary intake and exhaust vents are located along the sides of the chassis. Adequate clearance between the chassis and surrounding equipment or blockages must be maintained to ensure proper cooling of the chassis power supply as well as the modules plugged into the chassis. These clearances are outlined in Figure 2-1. The vent locations for the NI PXIe-1085 Series chassis are shown in Figure 2-2. Failure to provide these clearances may result in thermal-related failures in the chassis or modules.

Figure 2-1. NI PXIe-1085 Series Chassis Cooling Clearances

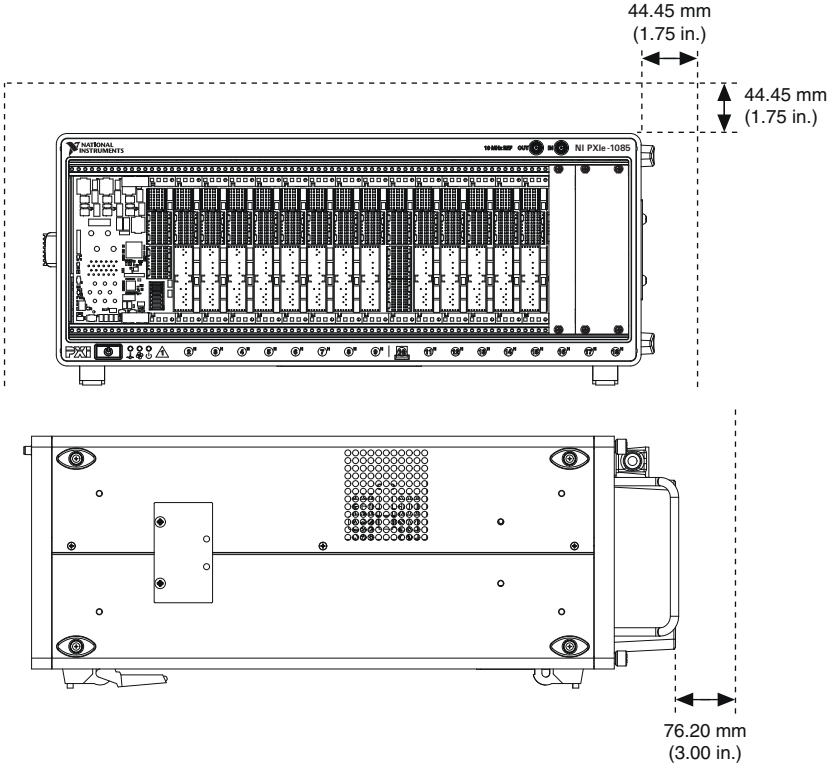
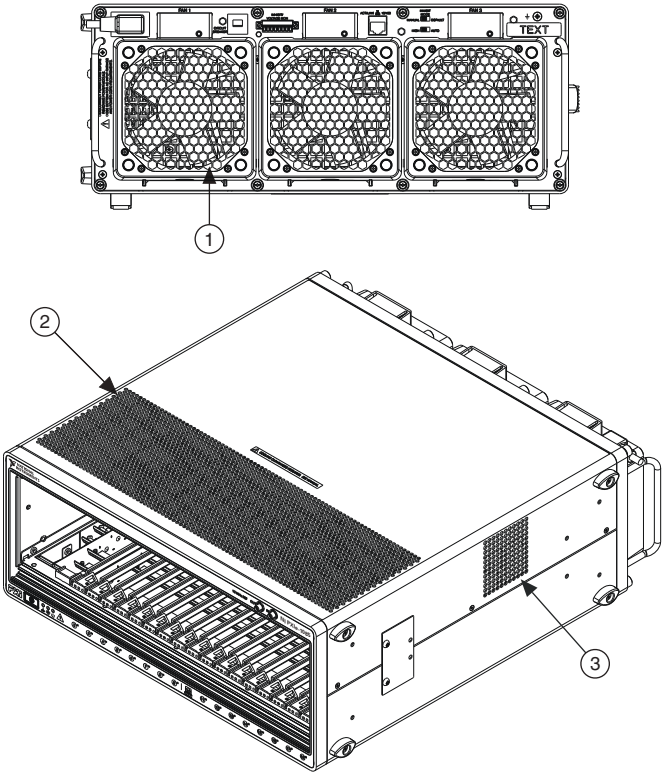


Figure 2-2. NI PXIe-1085 Series Chassis Vents



1	Primary Air Intake Vent (3x)	3	Secondary Air Intake/Exhaust Vents (Both Sides)
2	Primary Air Exhaust Vent		

Chassis Ambient Temperature Definition

The chassis fan control system uses intake air temperature as the input for controlling fan speeds when in Auto Fan Speed mode. Because of this, the chassis ambient temperature is defined as the temperature that exists just outside of the fan intake vents on the rear of the chassis. Note that this temperature may be higher than ambient room temperature depending on the surrounding equipment and/or blockages present. It is the user's responsibility to ensure that this ambient temperature does not exceed the rated ambient temperature as stated in Appendix A, *Specifications*. If the temperature exceeds the stated spec, the temperature LED blinks red, as discussed in the *Front Panel and Fan Module LED Indicators* section of this chapter.

Setting Fan Speed

The fan-speed selector switch is on the rear panel of the NI PXIe-1085 Series chassis. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, to locate the fan-speed selector switch. Select **High** for maximum cooling performance or **Auto** for improved acoustic performance. When set to **Auto**, the fan speed is determined by chassis intake air temperature.

Considerations for High Vibration Environment

For the best performance in a high vibration environment; tighten the modular power supply screws and the power supply shuttle mounting screws to 11.5 lb · in. (1.3 N · m) using a #2 Phillips screwdriver. See Figure 3-1, *Removing Power Supply Shuttle*, for screw locations.

Installing Filler Panels

To maintain proper module cooling performance, install filler panels (provided with the chassis) in unused or empty slots. Secure with the captive mounting screws provided.

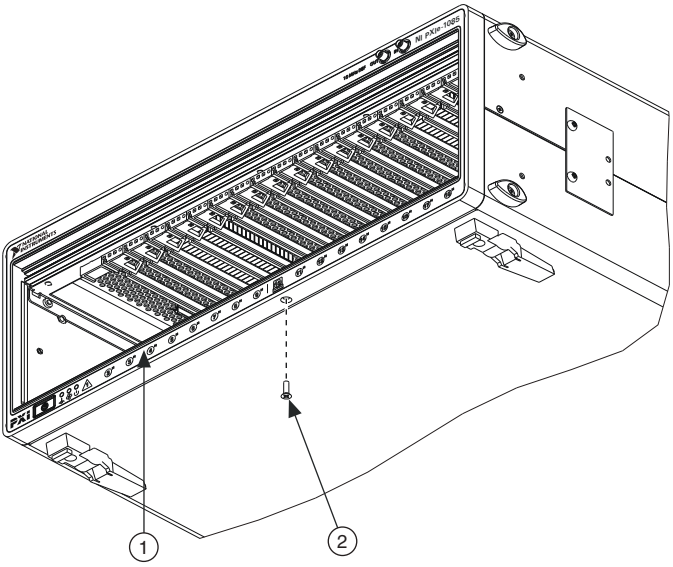
Installing Slot Blockers

The cooling performance of the chassis can be improved by installing optional slot blockers. Refer to `ni.com` for more details.

Securing Front Panel

To permanently secure the removable front panel, use the screw in the accessory kit. Attach the screw through the bottom of the front bezel using a #2 Phillips screwdriver, as shown in Figure 2-3.

Figure 2-3. Securing Removable Front Panel



1	Removable Front Panel	2	Screw to Secure Front Panel

Rack Mounting

Rack mount applications require the optional rack mount kits available from National Instruments. Refer to the instructions supplied with the rack mount kits to install your NI PXIe-1085 Series chassis in an instrument rack. Refer to Figure A-3, *NI Chassis Rack Mount Kit Components*.

Note You may want to remove the feet from the NI PXIe-1085 Series chassis when rack mounting. To do so, remove the screws holding the feet in place.

Connecting Safety Ground

Caution The NI PXIe-1085 Series chassis are designed with a three-position NEMA 5-15 style plug for the U.S. that connects the ground line to the chassis ground. To minimize shock hazard, make sure the electrical power outlet you use to power the chassis has an appropriate earth safety ground.

If your power outlet does not have an appropriate ground connection, you must connect the premise safety ground to the chassis grounding screw located on the rear panel. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, to locate the chassis grounding screw. To connect the safety ground, complete the following steps:

1. Connect a 16 AWG (1.3 mm) wire to the chassis grounding screw using a grounding lug. The wire must have green insulation with a yellow stripe or must be noninsulated (bare).
2. Attach the opposite end of the wire to permanent earth ground using toothed washers or a toothed lug.

Connecting to Power Source

Cautions Do *not* install modules prior to performing the following power-on test.

To completely remove power, you *must* disconnect the AC power cable.

Attach input power through the rear AC inlet using the appropriate AC power cable supplied. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, to locate the AC inlet.

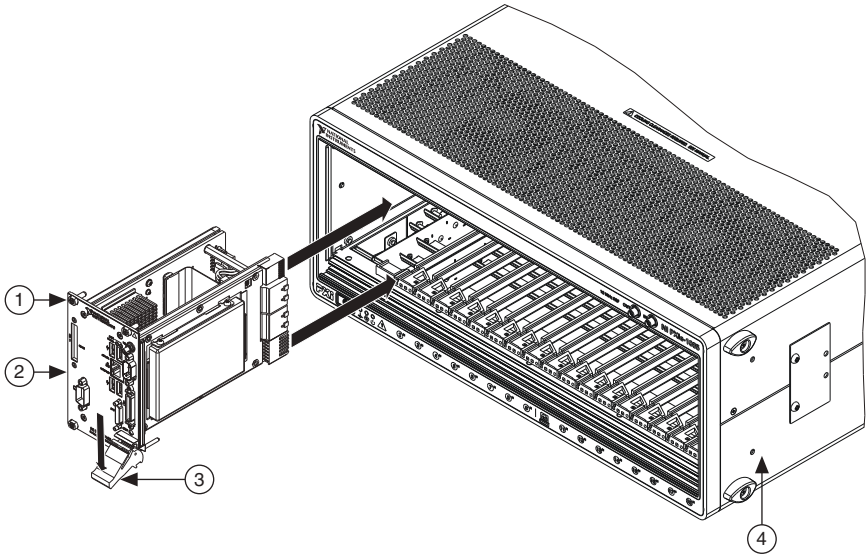
The Inhibit Mode switch allows you to power on the chassis or place it in standby mode. Set the Inhibit Mode switch on the back of the chassis to the **Manual** position. Observe that all fans become operational and all three front panel LEDs are a steady green. Switching the Inhibit Mode switch to the **Default** position allows the system controller to control the power supply.

Installing a PXI Express System Controller

This section contains general installation instructions for installing a PXI Express system controller in a NI PXIe-1085 Series chassis. Refer to your PXI Express system controller user manual for specific instructions and warnings. To install a system controller, complete the following steps:

1. Connect the AC power source to the PXI Express chassis before installing the system controller. The AC power cord grounds the chassis and protects it from electrical damage while you install the system controller.
2. Install the system controller into the system controller slot (slot 1, indicated by the red card guides) by first placing the system controller PCB into the front of the card guides (top and bottom). Slide the system controller to the rear of the chassis, making sure that the injector/ejector handle is pushed down as shown in Figure 2-4.

Figure 2-4. Installing a PXI Express System Controller

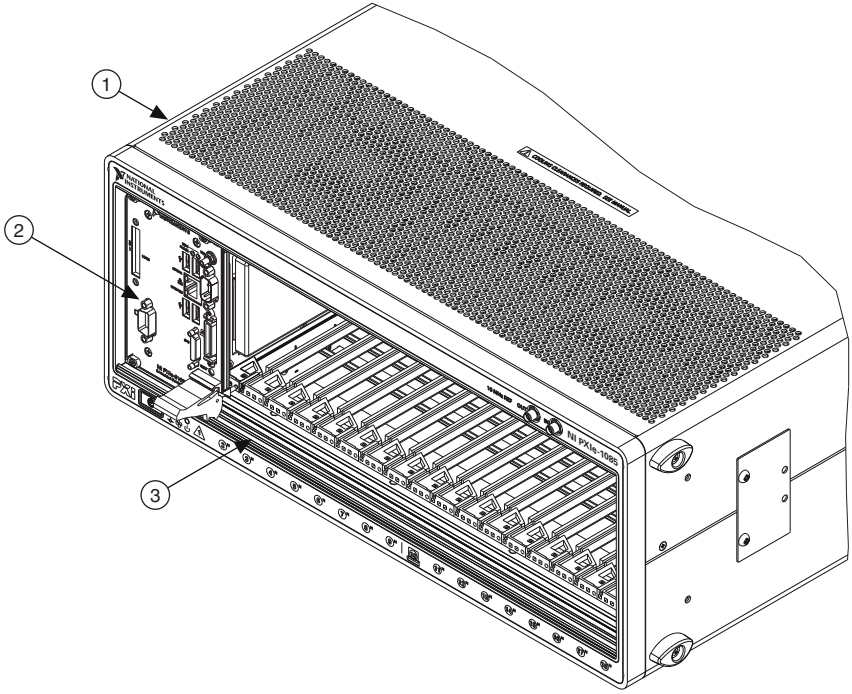


1	System Controller Front Panel Mounting Screws (4x)	3	Injector/Ejector Handle
2	NI PXI Express System Controller	4	NI PXIe-1085 Series Chassis

3. When you begin to feel resistance, pull up on the injector/ejector handle to seat the system controller fully into the chassis frame. Secure the system controller front panel to the chassis using the system controller front-panel mounting screws.
4. Connect the keyboard, mouse, and monitor to the appropriate connectors. Connect devices to ports as required by your system configuration.
5. Power on the chassis. Verify that the system controller boots. If the system controller does not boot, refer to your system controller user manual.

Figure 2-5 shows a PXI Express system controller installed in the system controller slot of a NI PXIe-1085 Series chassis. You can place CompactPCI, CompactPCI Express, PXI, or PXI Express modules in other slots depending on the slot type.

Figure 2-5. NI PXI Express System Controller Installed in a NI PXIe-1085 Series Chassis



1	NI PXIe-1085 Series Chassis	2	NI PXI Express System Controller	3	Injector/Ejector Rail

Installing Peripheral Modules

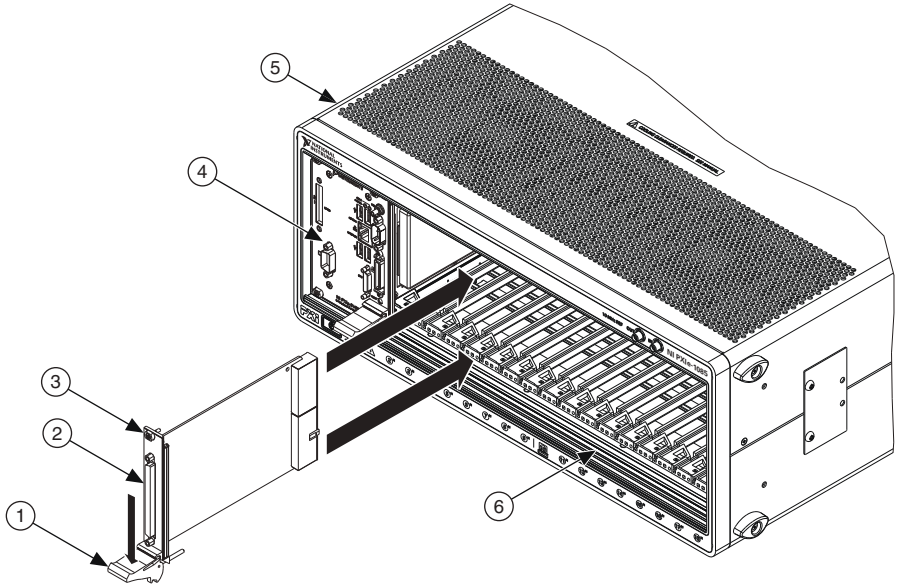
Caution The NI PXIe-1085 Series chassis has been designed to accept a variety of peripheral module types in different slots. To prevent damage to the chassis, ensure that the peripheral module is being installed into a slot designed to accept it. Refer to Chapter 1, *Getting Started*, for a description of the various slot types.

This section contains general installation instructions for installing a peripheral module in a NI PXIe-1085 Series chassis. Refer to your peripheral module user manual for specific instructions and warnings. To install a module, complete the following steps:

1. Connect the AC power source to the PXI Express chassis before installing the module. The AC power cord grounds the chassis and protects it from electrical damage while you install the module.
2. Ensure that the chassis is powered off.

3. Install a module into a chassis slot by first placing the module card PCB into the front of the card guides (top and bottom), as shown in Figure 2-6. Slide the module to the rear of the chassis, making sure that the injector/ejector handle is pushed down as shown in Figure 2-6.
4. When you begin to feel resistance, push up on the injector/ejector handle to fully seat the module into the chassis frame. Secure the module front panel to the chassis using the module front-panel mounting screws.

Figure 2-6. Installing PXI, PXI Express, or CompactPCI Peripheral Modules



1	Injector/Ejector Handle	4	NI PXI Express System Controller
2	PXI Peripheral Module	5	NI PXIe-1085 Series Chassis
3	Peripheral Module Front Panel Mounting Screws (2x)	6	Injector/Ejector Rail

Remote System Monitoring

The NI PXIe-1085 Series chassis provides an Ethernet port on the rear panel of the chassis. You can use this Ethernet port to monitor the chassis operating parameters remotely over a network. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, to locate the Ethernet connector.

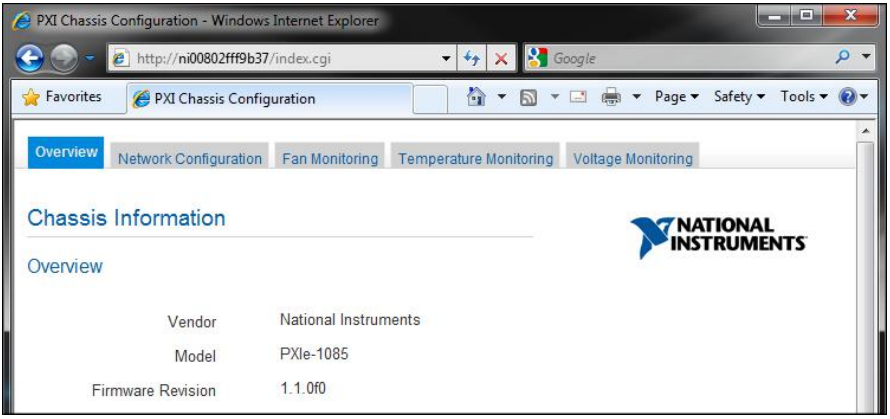
The Ethernet port on the chassis supports communication speeds of 10 Mbps and 100 Mbps. Contact your network administrator to determine whether your network supports DHCP. If your network uses DHCP, the network configuration is performed automatically.

To use the remote monitoring interface, connect one end of an Ethernet cable to your NI PXIe-1085 Series chassis. Connect the other end of the cable to your Ethernet network.

Note The Ethernet controller can perform automatic crossover, thus eliminating the need for crossover cables.

Through the remote monitoring Ethernet interface of the chassis, you can access a web page with information about the current chassis operating parameters. You can access this page in most browsers. Enter the IP address or hostname currently assigned to the chassis into the browser's address bar. Figure 2-7 shows an example of the web page.

Figure 2-7. Chassis Configuration Web Page



The Ethernet connector has two LEDs that indicate the current status of the Ethernet link. Table 2-1 describes the behavior of these LEDs.

Table 2-1. Ethernet LED Behavior

LED	State	Description
ACT/Link	Off	Link is not established.
	Steady green	Link is established.
	Blinking green	Chassis is communicating with another device on the network.
10/100	Off	10 Mbps data rate is selected.
	Steady green	100 Mbps data rate is selected

Default Configuration Settings

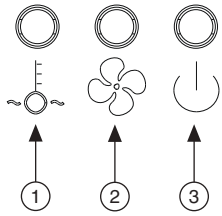
The chassis ships from the factory with the following default configuration settings:

- DHCP with Auto IP fallback
- Default hostname as printed on the product label

Front Panel and Fan Module LED Indicators

Figure 2-8 shows the front panel LEDs. Table 2-2 describes the LED states.

Figure 2-8. Front Panel LEDs



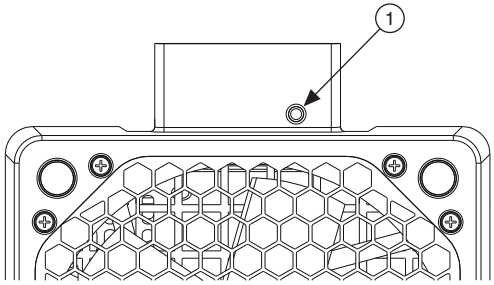
1 Temperature LED 2 Fan LED 3 Power LED

Table 2-2. Front Panel LED States

LED	State	Description
Temperature LED	Off	Chassis is powered off.
	Steady green	Intake temperature is within chassis operating range.
	Blinking red	Intake temperature is outside of chassis operating range.
	Steady red	Intake temperature has reached critical limits.
Fan LED	Off	Chassis is powered off.
	Steady green	All chassis fans are enabled and operating normally.
	Blinking red	A single chassis fan has failed, but chassis can continue to operate.
	Steady red	Two or more chassis fans have failed, and chassis must shut itself down.
Power LED	Off	Chassis is powered off.
	Steady green	Power supply is active, and all voltages are within normal operating ranges.
	Blinking red	Power supply is active, and at least one voltage is out of range.
	Steady red	Power supply has failed.

Figure 2-9 shows a fan module LED. Table 2-3 describes the LED states.

Figure 2-9. Fan Module LED



1 Fan Module LED

Table 2-3. Fan Module LED States

LED	State	Description
Fan module LED	Off	Chassis is powered off.
	Steady green	Fan is operating normally.
	Steady red	Fan has failed.

Note If two system fans or both of the power supply fans fail, the chassis shuts down automatically, preventing the chassis and modules from damage due to overheating.

Remote Voltage Monitoring and Control

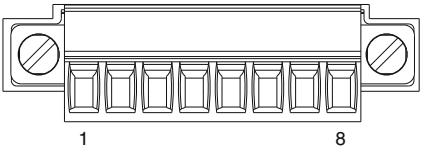
The NI PXIe-1085 Series chassis supports remote voltage monitoring and inhibiting through a female 8-pin connector on the rear panel. Table 2-4 shows the pinout of the 8-pin connector.

Note The NI PXIe-1085 Series chassis accessory kit includes one 8-pin connector. To order additional connectors, use Phoenix Contact part number MC 1.5/8-STF-3.5-BK or 1847181.

Caution The Inhibit/Voltage Mon port can be damaged if subjected to Electrostatic Discharge (ESD). To prevent damage, industry-standard ESD prevention measures must be employed during installation, maintenance, and operation.

Table 2-4. Remote Inhibit and Voltage Monitoring Connector Pinout

Pin	Signal
1	Inhibit (Active Low)
2	Fault (Active High)
3	Logic Ground
4	+5 VDC
5	+3.3 VDC
6	+12 VDC
7	-12 VDC
8	Logic Ground



Caution When connecting digital voltmeter probes to the rear 8-pin connector, be careful not to short the probe leads together.

You can use a digital voltmeter to ensure all voltage levels in the NI PXIe-1085 Series chassis are within the allowable limits. Referring to Table 2-5, connect one lead of the voltmeter to a supply pin on the 8-pin remote voltage monitoring connector on the rear panel. Refer to Table 2-4 for a pinout diagram of the remote voltage monitoring connector. Connect the reference lead of the voltmeter to one of the ground pins. Compare each voltage reading to the values listed in Table 2-5.

Note Use the rear-panel 8-pin connector to check voltages only. Do not use the connector to supply power to external devices.

Table 2-5. Power Supply Voltages at Voltage Monitoring Connector

Pin	Supply	Acceptable Voltage Range
4	+5 V	4.75 to 5.25 V
5	+3.3 V	3.135 to 3.465 V
6	+12 V	11.4 to 12.6 V
7	-12 V	-12.6 to -11.4 V
3, 8	Logic Ground	0 V

If the voltages fall within the specified ranges, the chassis complies with the CompactPCI voltage-limit specifications.

Inhibit Mode Switch

On the rear panel of the chassis there is an Inhibit Mode switch. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, for the location.

The Inhibit Mode switch should be in the **Default** position when normal power inhibit switch functionality is desired. If the user needs to power on a chassis without a system controller installed the switch should be in the **Manual** position.

When the Inhibit Mode switch is set to the **Manual** position, the power supplies are enabled, and you can use the Inhibit signal (active low) on pin 1 of the Remote Inhibit and Voltage Monitoring connector to power off the chassis. To remotely power off the chassis, connect the Inhibit pin (pin 1) to a Logic Ground pin (pin 3 or 8). As long as this connection exists, the chassis will remain off (standby); when you remove this connection, the chassis turns on.

Note For the Remote Inhibit signal to control the On/Off (standby) state of the chassis, the Inhibit Mode switch must be in the **Manual** position.

PXI_CLK10 Front Panel Connectors

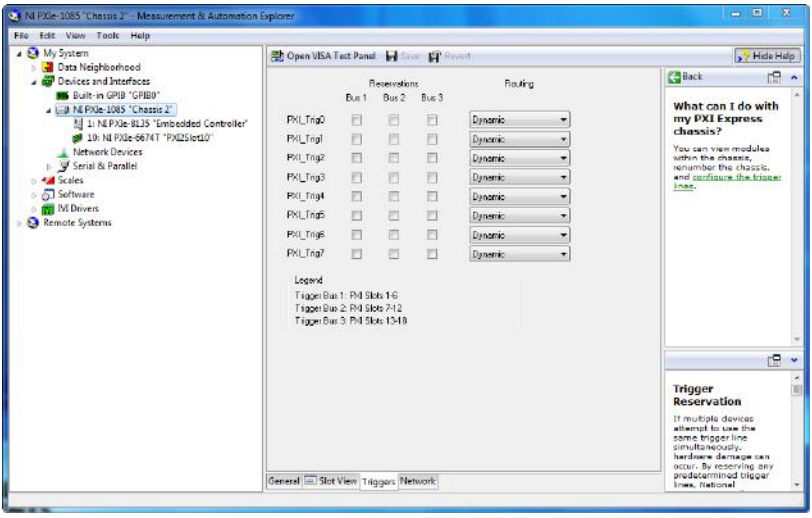
There are two SMA connectors on the front of the NI PXIe-1085 Series chassis for PXI_CLK10. The connectors are labeled IN and OUT. You can use them for supplying the backplane with PXI_CLK10 or routing the backplane's PXI_CLK10 to another chassis. Refer to the *System Reference Clock* section of Chapter 1, *Getting Started*, for details about these signals.

PXI Express System Configuration with MAX

The PXI Platform Services software included with your chassis automatically identifies your PXI Express system components to generate a `pxiesys.ini` file. You can configure your entire PXI system and identify PXI-1 chassis through Measurement & Automation Explorer (MAX), included with your system controller. MAX creates the `pxiesys.ini` and `pxisys.ini` file, which define your PXI system parameters. MAX also provides an interface to route and reserve triggers so dynamic routing, through drivers such as DAQmx, avoids double-driving and potentially damaging trigger lines. For more information about routing and reserving PXI triggers, refer to KnowledgeBase 3TJDOND8 at `ni.com/support`.

The configuration steps for single or multiple-chassis systems are the same.

Figure 2-10. Multichassis Configuration in MAX



PXI-1 System Configuration

1. Launch MAX.
2. In the **Configuration** tree, click the **Devices and Interfaces** branch to expand it.
3. If the PXI system controller has not yet been configured, it is labeled **PXI System (Unidentified)**. Right-click this entry to display the pop-up menu, then select the appropriate system controller model from the **Identify As** submenu.
4. Click the PXI system controller. The chassis (or multiple chassis, in a multichassis configuration) is listed below it. Identify each chassis by right-clicking its entry, then selecting the appropriate chassis model through the **Identify As** submenu. Further expanding the **PXI System** branch shows all devices in the system that can be recognized by NI-VISA. When your system controller and all your chassis are identified, the required `pxisys.ini` file is complete.

The PXI specification allows for many combinations of PXI chassis and system modules. To assist system integrators, the manufacturers of PXI chassis and system modules must document the capabilities of their products. PXI Express devices must provide a driver and `.ini` file for identification. These files are provided as part of the PXI Platform Services software included with your system controller. The minimum documentation requirements for PXI-1 are contained in `.ini` files, which consist of ASCII text. System integrators, configuration utilities, and device drivers can use these `.ini` files.

The capability documentation for a PXI-1 chassis is contained in a `chassis.ini` file provided by the chassis manufacturer. The information in this file is combined with information about the system controller to create a single PXI-1 system initialization file called `pxisys.ini` (PXI System Initialization). The NI system controller uses MAX to generate the `pxisys.ini` file from the `chassis.ini` file.

Device drivers and other utility software read the `pxiesys.ini` and `pxisys.ini` file to obtain system information. For detailed information about initialization files, refer to the PXI specification at `www.pxisa.org`.

Trigger Configuration in MAX

Each chassis has one or more trigger buses, each with eight lines numbered 0 through 7 that can be reserved and routed statically or dynamically. Static reservation *pre-allocates* a trigger line to prevent its configuration by a user program. Dynamic reservation/routing/deallocation is *on the fly* within a user program based upon National Instruments APIs such as NI-DAQmx. Static reservation of trigger lines can be implemented by the user in MAX through the **Triggers** tab. Reserved trigger lines will not be used by PXI modules dynamically configured by programs such as NI-DAQmx. This prevents the instruments from double-driving the trigger lines, possibly damaging devices in the chassis. In the default configuration, trigger lines on each bus are independent. For example, if trigger line 3 is asserted on trigger bus 0, by default it will not be automatically asserted on any other trigger bus.

Complete the following steps to reserve these trigger lines in MAX.

1. In the Configuration tree, click on the PXI chassis branch you want to configure.
2. Then, in the right-hand pane, toward the bottom, click on the **Triggers** tab.
3. Select which trigger lines you would like to statically reserve.
4. Click the **Save** button.

PXI Trigger Bus Routing

Some National Instruments chassis, such as the NI PXIe-1085 Series and the NI PXI-1044/1045, have the capability to route triggers from one bus to others within the same chassis using the **Trigger Routing** tab in MAX, as shown in Figure 2-10.

Note Selecting any non-disabled routing automatically reserves the line in all trigger buses being routed to. If you are using NI-DAQmx, it will reserve and route trigger lines for you, so you won't have to route trigger lines manually.

Complete the following steps to configure trigger routings in MAX.

1. In the **Configuration** tree, select the chassis in which you want to route trigger lines.
2. In the right-hand pane, select the **Trigger Routing** tab near the bottom.
3. For each trigger line, select **Route Right**, **Route Outward From Middle**, or **Route Left** to route triggers on that line in the described direction, or select **Disabled** for the default behavior with no manual routing.
4. Click the **Apply** button.

Using System Configuration and Initialization Files

The PXI Express specification allows many combinations of PXI Express chassis and system modules. To assist system integrators, the manufacturers of PXI Express chassis and system modules must document the capabilities of their products. The minimum documentation requirements are contained in `.ini` files, which consist of ASCII text. System integrators, configuration utilities, and device drivers can use these `.ini` files.

The capability documentation for the NI PXIe-1085 Series chassis is contained in the `chassis.ini` file on the software media that comes with the chassis. The information in this file is combined with information about the system controller to create a single system initialization file called `pxisys.ini` (PXI System Initialization). The system controller manufacturer either provides a `pxisys.ini` file for the particular chassis model that contains the system controller or provides a utility that can read an arbitrary `chassis.ini` file and generate the corresponding `pxisys.ini` file. System controllers from NI provide the `pxisys.ini` file for the NI PXIe-1085 Series chassis, so you should not need to use the `chassis.ini` file. Refer to the documentation provided with the system controller or to `ni.com/support` for more information on `pxisys.ini` and `chassis.ini` files.

Device drivers and other utility software read the `pxisys.ini` file to obtain system information. The device drivers should have no need to directly read the `chassis.ini` file. For detailed information regarding initialization files, refer to the PXI Express specification at `www.pxisa.org`.

3 Maintenance

This chapter describes basic maintenance procedures you can perform on the NI PXIe-1085 Series chassis.

Caution Disconnect the power cable prior to servicing a NI PXIe-1085 Series chassis.

Service Interval

Clean dust from the chassis exterior (and interior) as needed, based on the operating environment. Periodic cleaning increases reliability.

Preparation

The information in this section is designed for use by qualified service personnel. Read the *Read Me First: Safety and Electromagnetic Compatibility* document included with your kit before attempting any procedures in this chapter.

Caution Many components within the chassis are susceptible to static discharge damage. Service the chassis only in a static-free environment. Observe standard handling precautions for static-sensitive devices while servicing the chassis. *Always* wear a grounded wrist strap or equivalent while servicing the chassis.

Cleaning

Cleaning procedures consist of exterior and interior cleaning of the chassis. Refer to your module user documentation for information on cleaning the individual CompactPCI or PXI Express modules.

Caution *Always* disconnect the AC power cable before cleaning or servicing the chassis.

Interior Cleaning

Use a dry, low-velocity stream of air to clean the interior of the chassis. Use a soft-bristle brush for cleaning around components.

Exterior Cleaning

Clean the exterior surfaces of the chassis with a dry lint-free cloth or a soft-bristle brush. If any dirt remains, wipe with a cloth moistened in a mild soap solution. Remove any soap residue by wiping with a cloth moistened with clear water. Do not use abrasive compounds on any part of the chassis.

Cautions Avoid getting moisture inside the chassis during exterior cleaning, especially through the top vents. Use just enough moisture to dampen the cloth.

Do *not* wash the front- or rear-panel connectors or switches. Cover these components while cleaning the chassis.

Do *not* use harsh chemical cleaning agents; they may damage the chassis. Avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.

Resetting the AC Mains Circuit Breaker

If the NI PXIe-1085 Series chassis is connected to an AC source and encounters an over-current condition, the circuit breaker on the rear panel will trip to prevent damage to the chassis. Complete the following steps to reset the circuit breaker.

1. Turn off the chassis.
2. Disconnect the AC power cable.
3. Depress the circuit breaker to reset it.
4. Reconnect the AC power cable.
5. Turn on the chassis.

If the circuit breaker trips again, complete the following steps:

1. Turn off the chassis.
2. Disconnect the AC power cable.
3. Remove all modules from the chassis.
4. Complete the procedure described in the *Connecting to Power Source* section of Chapter 2, *Installation and Configuration*. If the power switch LED is not a steady green, contact National Instruments.
5. Verify that the NI PXIe-1085 Series chassis can meet the power requirements of your CompactPCI or PXI Express modules. Overloading the chassis can cause the breaker to trip. Refer to Appendix A, *Specifications*.
6. The over-current condition that caused the circuit breaker to trip may be due to a faulty CompactPCI or PXI Express module. Refer to the documentation supplied with the modules for troubleshooting information.

Replacing the Modular Power Supply

This section describes how to remove, configure, and install the AC power supply shuttle in the NI PXIe-1085 Series chassis.

Caution Disconnect the power cable prior to replacing the power supply.

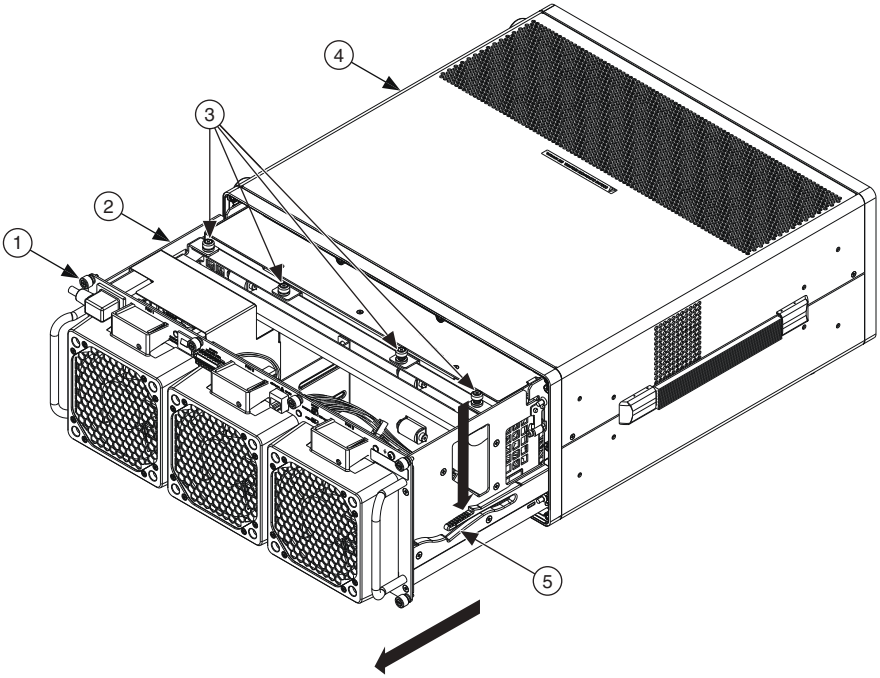
Before connecting the power supply shuttle to a power source, read this section and the *Read Me First: Safety and Electromagnetic Compatibility* document included with the kit.

Removal

The NI PXIe-1085 Series power supply is a replacement part for the NI PXIe-1085 Series chassis. Before attempting to replace the power supply, verify that there is adequate clearance behind the chassis. Disconnect the power cable from the power supply shuttle on the back of the chassis. Identify the eight mounting screws for the chassis that attach the power supply shuttle to the chassis. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, for the screw locations. Using a Phillips screwdriver, remove the screws. Pull on the two rear handles of the power supply shuttle to remove it from the back of the chassis, as shown in Figure 3-1. About halfway through removing the shuttle, the shuttle rail safety catches engage to prevent the shuttle from falling out. Press down on the shuttle rail safety catches to remove the shuttle the rest of the way, as shown in Figure 3-1.

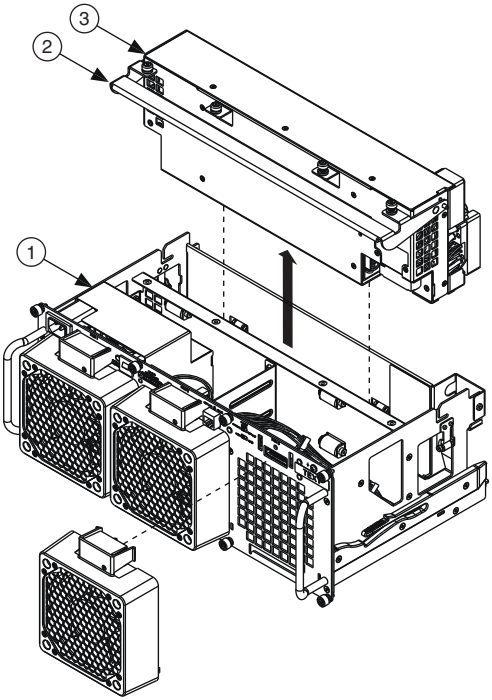
After removing the shuttle from the chassis, you can access the modular power supply. To remove the modular power supply, first loosen the four screws that retain it. Refer to Figure 3-1 for the screw locations. After loosening the screws, you can remove the modular power supply by rotating the handle away from the fans and pulling upward when it is in the upright position, as shown in Figure 3-2.

Figure 3-1. Removing Power Supply Shuttle



1	Power Supply Shuttle Mounting Screws (8x)	4	NI PXIe-1085 Series Chassis
2	Power Supply Shuttle	5	Shuttle Rail Safety Catch (Both Sides)
3	Modular Power Supply Screws (4x)		

Figure 3-2. Removing Modular Power Supply from Power Supply Shuttle



1	Power Supply Shuttle	2	Modular Power Supply Handle	3	Modular Power Supply

Installation

Ensure that there is no visible damage to the new power supply assembly. Verify that the housing and connector on the new power supply assembly have no foreign material inside. Install the new power supply assembly into the opening in the shuttle in the reverse order of removal. Replace and tighten the four screws with a Phillips screwdriver or by hand.

After installing the power supply assembly, slide the power supply shuttle into the opening in the rear of the chassis. Tighten the eight screws with a Phillips screwdriver.

Configuration

The fan-speed selector switch is on the rear panel of the power supply shuttle. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, to locate the fan-speed selector. Select **High** for maximum cooling performance (recommended) or **Auto** for quieter operation. Set the Inhibit Mode switch to the **Default** position.

Connecting Safety Ground

Refer to the *Connecting Safety Ground* section of Chapter 2, *Installation and Configuration*.

Connecting to Power Source

Refer to the *Connecting to Power Source* section of Chapter 2, *Installation and Configuration*.

Installing Replacement Fan Modules

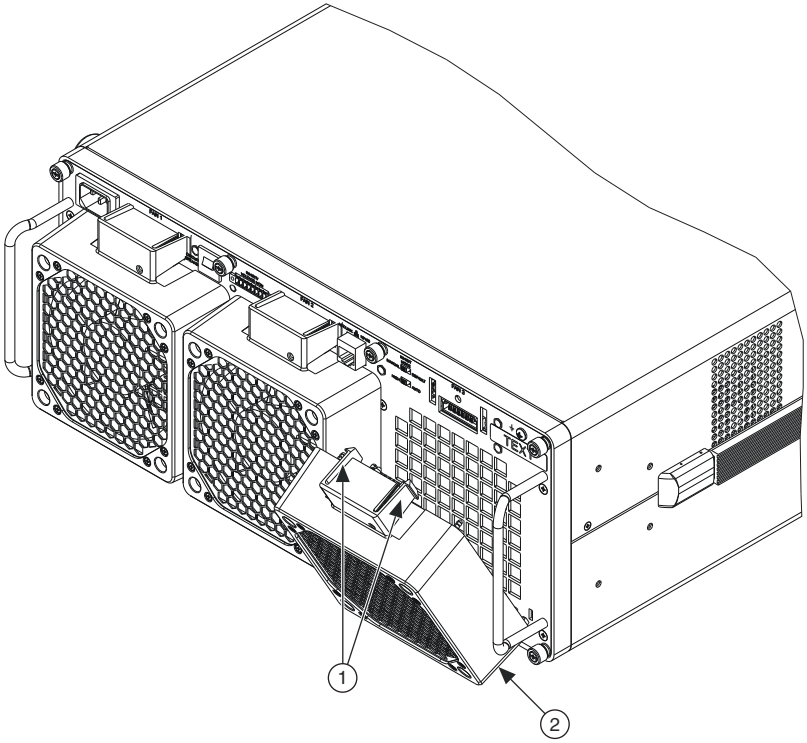
Follow these steps to remove a failed fan module:

1. Pinch both snaps at the top of the fan module simultaneously.
2. Rotate the fan module downwards and remove from the chassis, as shown in Figure 3-3.

Follow these steps to install a new fan module:

1. Insert the tab that projects from the bottom of the fan module into the slot on the back of the chassis. Be sure the tab catches on the bottom of the slot.
2. Rotate the fan module upwards.
3. Pinch both snaps at the top of the fan module, rotate the module until it is flush with the chassis, and release the snaps.

Figure 3-3. Replacing Fan Module



1	Fan Module Snaps	2	Fan Module

A

Specifications

This appendix contains specifications for the NI PXIe-1085 Series chassis.

Caution Specifications are subject to change without notice.

Electrical

AC Input

Input voltage range ..... 100 VAC to 240 VAC

Operating voltage range[1] ..... 90 VAC to 264 VAC

Input frequency ..... 50 Hz/60 Hz

Operating frequency range[1] ..... 47 Hz to 63 Hz

Input current rating ..... 12 A to 6 A

Over-current protection ..... 15 A circuit breaker

Line regulation

- 3.3 V ..... <±0.2%
- 5 V ..... <±0.1%
- ±12 V ..... <±0.1%

Efficiency ..... 70% typical

Power disconnect ..... The AC power cable provides main power disconnect. Do not position the equipment so that it is difficult to disconnect the power cord. The front-panel power switch causes the internal chassis power supply to provide DC power to the CompactPCI/PXI Express backplane. You also can use the rear-panel 8-pin connector and inhibit mode switch to control the internal chassis power supply.

[1] The operating range is guaranteed by design.

DC Output

DC current capacity (I_{MP})

Voltage	Maximum Current	
	NI PXIe-1085 12 GB/s	NI PXIe-1085 24 GB/s
+3.3 V	60 A	60 A
+5 V	44 A	49 A
+12 V	62 A	62 A
-12 V	4 A	4 A
5 VAUX	2 A	2 A

Note Maximum total available power for the NI PXIe-1085 12 GB/s is 791 W.

Maximum total available power for the NI PXIe-1085 24 GB/s is 775 W.

Backplane slot current capacity

Slot	+5 V	V(I/O)	+3.3 V	+12 V	-12 V	5 VAUX
System Controller Slot	15 A	—	15 A	30 A	—	1 A
System Timing Slot	—	—	6 A	4 A	—	1 A
Hybrid Peripheral Slot with PXI-1 Peripheral	6 A	5 A	6 A	1 A	1 A	—
Hybrid Peripheral Slot with PXI-5 Peripheral	—	—	6 A	4 A	—	1 A
PXI-1 Peripheral Slot	6 A	11 A	6 A	1 A	1 A	—

Notes Total system slot current should not exceed 45 A.

PCI V(I/O) pins in PXI-1 peripheral slots and hybrid peripheral slots are connected to +5 V.

The maximum power dissipated in the system slot should not exceed 140 W.

The maximum power dissipated in a peripheral slot should not exceed 38.25 W.

Load regulation

Voltage	Load Regulation
+3.3 V	<5%
+12 V	<5%
+5 V	<5%
-12 V	<5%

Maximum ripple and noise (20 MHz bandwidth)

Voltage	Maximum Ripple and Noise
+3.3 V	50 mVpp
+12 V	50 mVpp
+5 V	50 mVpp
-12 V	50 mVpp

Over-current protection ..... All outputs protected from short circuit and overload with automatic recovery

Over-voltage protection

3.3 V and 5 V..... Clamped at 20 to 30% above nominal output voltage

Power supply shuttle MTTR..... Replacement in under 5 minutes

Remote Inhibit and Voltage Monitoring Connector

Fault output signal

VOH..... 3.8 V (I_{OH} = -8 mA)

VOL ..... 0.44 V (I_{OH} = 8 mA)

Inhibit input signal

VIH ..... 3.5 V (min)

VIL..... 1.5 V (max)

Note Internal 10 kΩ pull-up to 5 VAUX.

Chassis Cooling

Module cooling system

NI PXIe-1085 Series chassis.....Forced air circulation (positive pressurization) through three 169 cfm fans with High/Auto speed selector

Slot airflow direction .....Bottom of module to top of module

Module cooling intake .....Bottom rear of chassis

Module cooling exhaust.....Along both sides and top of chassis

Power supply cooling system .....Forced air circulation through two integrated fans

Power supply cooling intake.....Right side of chassis

Power supply cooling exhaust .....Left side of chassis

Environmental

Maximum altitude.....2,000 m (800 mbar) (at 25 °C ambient)

Pollution Degree 2

For indoor use only.

Operating Environment

Ambient temperature range .....0 to 55 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)

Relative humidity range.....10 to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range .....-40 to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)

Relative humidity range.....5 to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operational shock ..... 30 g peak, half-sine, 11 ms pulse
(Tested in accordance with IEC 60068-2-27.
Meets MIL-PRF-28800F Class 2 limits.)

Random Vibration..... 5 to 500 Hz, 0.3 g_{rms}

Acoustic Emissions

Sound Pressure Level (at Operator Position)

(Tested in accordance with ISO 7779. Meets MIL-PRF-28800F requirements.)

Auto fan (up to ~30 °C ambient) ..... 51.2 dBA

High fan ..... 64.1 dBA

Sound Power

Auto fan (up to ~30 °C ambient) ..... 60.8 dBA

High fan ..... 75.9 dBA

Caution The protection provided by the NI PXIe-1085 Series can be impaired if it is used in a manner not described in this document.

Note Specifications are subject to change without notice.

Safety

This product is designed to meet the requirements of the following standards of safety for information technology equipment:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions

- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations and certifications, and additional information, refer to the *Online Product Certification* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

Backplane

Size ..... 3U-sized; one system slot (with three system expansion slots) and 17 peripheral slots. Compliant with IEEE 1101.10 mechanical packaging. PXI Express Specification compliant. Accepts both PXI Express and CompactPCI (PICMG 2.0 R 3.0) 3U modules.

Backplane bare-board material ..... UL 94 V-0 Recognized

Backplane connectors ..... Conforms to IEC 917 and IEC 1076-4-101, and are UL 94 V-0 rated

System Synchronization Clocks (PXI_CLK10, PXIe_CLK100, PXIe_SYNC100)

10 MHz System Reference Clock: PXI_CLK10

Maximum slot-to-slot skew ..... 1 ns

Accuracy ..... ±25 ppm max. (guaranteed over the operating temperature range)

Maximum jitter ..... 5 ps RMS phase-jitter (10 Hz to 1 MHz range)

Duty-factor ..... 45% to 55%

Unloaded signal swing ..... 3.3 V ±0.3 V

Note For other specifications refer to the *PXI-1 Hardware Specification*.

100 MHz System Reference Clock: PXIe_CLK100 and PXIe_SYNC100

Maximum slot-to-slot skew ..... 100 ps

Accuracy ..... ±25 ppm max. (guaranteed over the operating temperature range)

Maximum jitter ..... 3 ps RMS phase-jitter (10 Hz to 12 kHz range); 2 ps RMS phase-jitter (12 kHz to 20 MHz range)

Duty-factor for PXIe_CLK100 ..... 45% to 55%

Absolute single-ended voltage swing (When each line in the differential pair has 50 W termination to 1.30 V or Thévenin equivalent) ..... 400 mV to 1000 mV

Note For other specifications refer to the *PXI-5 PXI Express Hardware Specification*.

External 10 MHz Reference Out (SMA on front panel of chassis)

Accuracy ..... ±25 ppm max. (guaranteed over the operating temperature range)

Maximum jitter ..... 5 ps RMS phase-jitter (10 Hz to 1 MHz range)

Output amplitude ..... 1 VPP ±20% square-wave into 50 Ω
2 VPP unloaded

Output impedance ..... 50 Ω ±5 Ω

External Clock Source

Frequency ..... 10 MHz ±100 PPM

Input amplitude

- Rear panel BNC ..... 200 mVPP to 5 VPP square-wave or sine-wave
- System timing slot PXI_CLK10_IN ..... 5 V or 3.3 V TTL signal

Front panel SMA input impedance ..... 50 Ω ±5 Ω

Maximum jitter introduced by backplane ..... 1 ps RMS phase-jitter (10 Hz to 1 MHz range)

PXIe_SYNC_CTRL

VIH ..... 2.0 V to 5.5 V

VIL ..... 0 V to 0.8 V

PXI Star Trigger

Maximum slot-to-slot skew ..... 250 ps

Backplane characteristic impedance ..... 65 Ω ±10%

Notes For PXI slot to PXI Star mapping refer to the *NI PXIe-1085 24 GB/s PCI Express Backplane Diagram* section of Chapter 1, *Getting Started*.

For other specifications refer to the *PXI-1 Hardware Specification*.

PXI Differential Star Triggers (PXIe-DSTARA, PXIe-DSTARB, PXIe-DSTARC)

Maximum slot-to-slot skew ..... 150 ps

Maximum differential skew..... 25 ps

Backplane differential impedance ..... 100 Ω ±10%

Notes For PXI Express slot to PXI_DSTAR mapping refer to the *NI PXIe-1085 24 GB/s PCI Express Backplane Diagram* section of Chapter 1, *Getting Started*.

For other specifications, the NI PXIe-1085 Series chassis complies with the *PXI-5 PXI Express Hardware Specification*.

Mechanical

Overall dimensions

Standard chassis

Height ..... 6.97 in. (177.1 mm)

Width ..... 18.30 in. (464.8 mm)

Depth ..... 19.38 in. (492.3 mm)

Note 0.57 in. (14.5 mm) is added to height when feet are installed. When tilted with front feet extended on table top, height is increased approximately 2.08 in. (52.8 mm) in front and 0.583 in. (14.8 mm) in rear.

Weight..... 40.3 lb (18.28 kg)

Chassis materials ..... Sheet Aluminum (5052-H32, 5754-H22), Extruded Aluminum (6063-T5, 6060-T6), Plate Aluminum (6063-T5, 6061-T6), Cold Rolled Steel, Cold Rolled Stainless Steel, Sheet Copper (C110), Santoprene, Urethane Foam, PC-ABS, Nylon, Polycarbonate, Delrin, Polyethylene, Polyamide (FR-106), Neodymium Magnet

Finish ..... Conductive Clear Iridite on Aluminum, Electroplated Nickel on Cold Rolled Steel, Electroplated Zinc on Cold Rolled Steel, Electroplated Nickel on Copper

Figures A-1 and A-2 show the NI PXIe-1085 Series chassis dimensions. The holes shown are for the installation of the optional rack mount kits. You can install those kits on the front or rear of the chassis, depending on which end of the chassis you want to face toward the front of the instrument cabinet. Notice that the front and rear chassis mounting holes (size M4) are symmetrical.

Figure A-1. NI PXIe-1085 Series Chassis Dimensions (Front and Side)

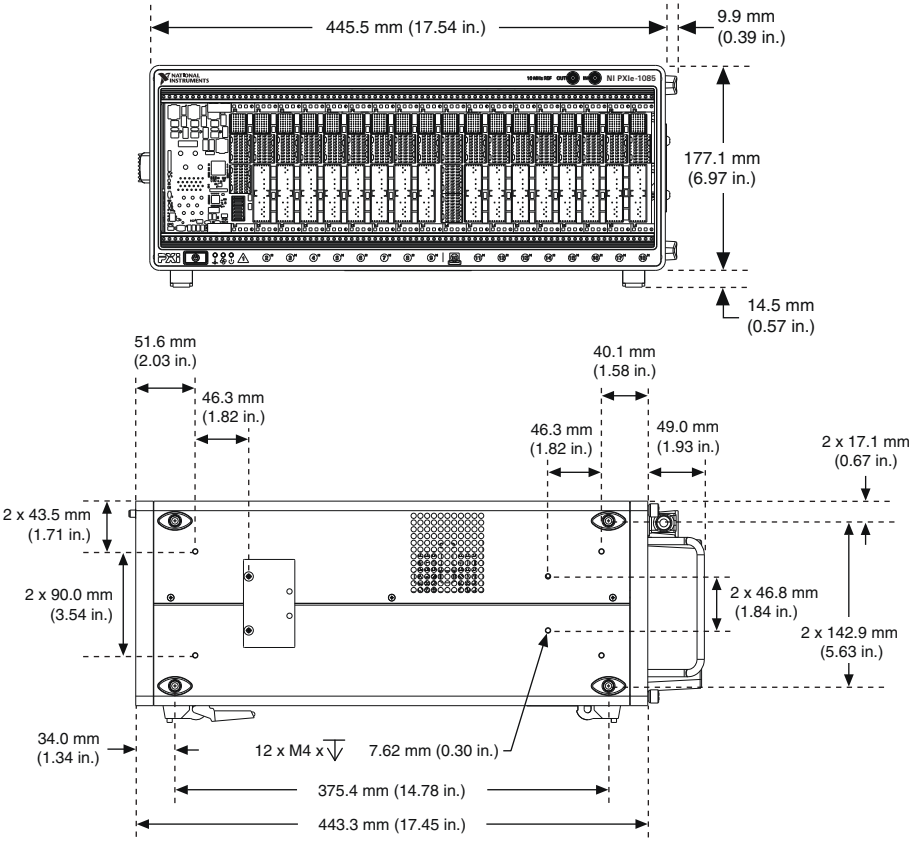


Figure A-2. NI PXIe-1085 Series Chassis Dimensions (Bottom)

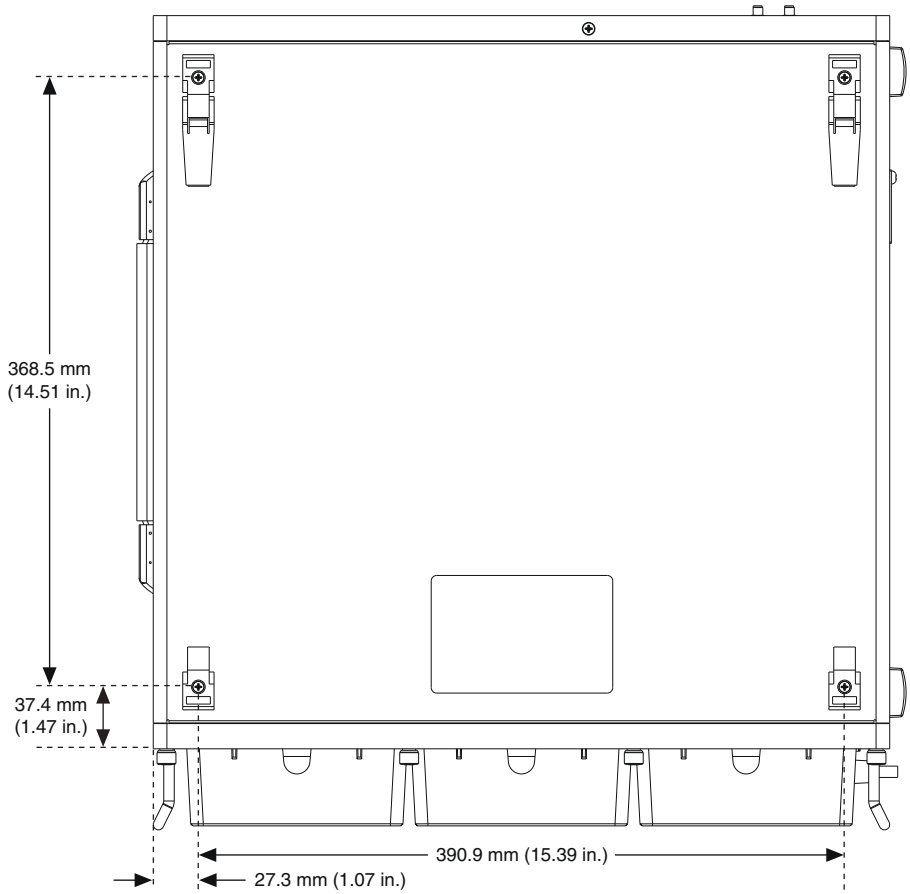
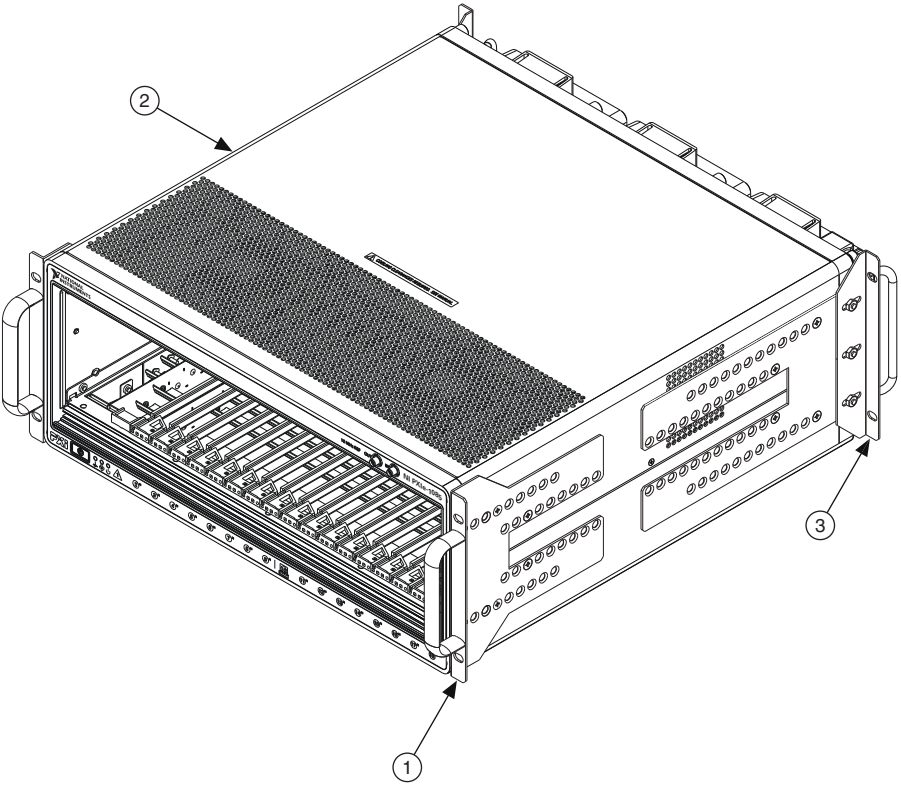


Figure A-3 shows the chassis rack mount kit components.

Figure A-3. NI Chassis Rack Mount Kit Components



1	Front Rack Mount Kit	2	NI PXIe-1085 Series Chassis	3	Rear Rack Mount Kit

B

Pinouts

This appendix describes the connector pinouts for the NI PXIe-1085 Series chassis backplane.

Table B-1 shows the XP1 Connector Pinout for the System Controller slot.

Table B-2 shows the XP2 Connector Pinout for the System Controller slot.

Table B-3 shows the XP3 Connector Pinout for the System Controller slot.

Table B-4 shows the XP4 Connector Pinout for the System Controller slot.

Table B-5 shows the TP1 Connector Pinout for the System Controller slot.

Table B-6 shows the TP2 Connector Pinout for the System Timing slot.

Table B-7 shows the XP3 Connector Pinout for the System Timing slot.

Table B-8 shows the XP4 Connector Pinout for the System Timing slot.

Table B-9 shows the P1 Connector Pinout for the peripheral slots.

Table B-10 shows the P2 Connector Pinout for the peripheral slots.

Table B-11 shows the P1 Connector Pinout for the Hybrid peripheral slots.

Table B-12 shows the XP3 Connector Pinout for the Hybrid peripheral slots.

Table B-13 shows the XP4 Connector Pinout for the Hybrid peripheral slots.

For more detailed information, refer to the *PXI-5 PXI Express Hardware Specification*, Revision 2.0. Contact the PXI Systems Alliance for a copy of the specification.

System Controller Slot Pinouts

Table B-1. XP1 Connector Pinout for the System Controller Slot

Pins	Signals
A	GND
B	12V
C	12V
D	GND
E	5V
F	3.3V
G	GND

Table B-2. XP2 Connector Pinout for the System Controller Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	2PETp1	2PETn1	GND	2PERp1	2PERn1	GND	2PETp2	2PETn2	GND
2	2PETp3	2PETn3	GND	2PERp3	2PERn3	GND	2PERp2	2PERn2	GND
3	2PETp4	2PETn4	GND	2PERp4	2PERn4	GND	2PETp5	2PETn5	GND
4	2PETp6	2PETn6	GND	2PERp6	2PERn6	GND	2PERp5	2PERn5	GND
5	2PETp7	2PETn7	GND	2PERp7	2PERn7	GND	2PETp8	2PETn8	GND
6	2PETp9	2PETn9	GND	2PERp9	2PERn9	GND	2PERp8	2PERn8	GND
7	2PETp10	2PETn10	GND	2PERp10	2PERn10	GND	2PETp11	2PETn11	GND
8	2PETp12	2PETn12	GND	2PERp12	2PERn12	GND	2PERp11	2PERn11	GND
9	2PETp13	2PETn13	GND	2PERp13	2PERn13	GND	2PETp14	2PETn14	GND
10	2PETp15	2PETn15	GND	2PERp15	2PERn15	GND	2PERp14	2PERn14	GND

Table B-3. XP3 Connector Pinout for the System Controller Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
2	RSV	RSV	GND	PWR_OK	PS_ON#	GND	LINKCAP	PWRBTN#	GND
3	SMBDAT	SMBCLK	GND	RSVD	RSVD	GND	RSVD	RSVD	GND
4	RSV	PERST#	GND	2RefClk+	2RefClk-	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	2PETp0	2PETn0	GND	2PERp0	2PERn0	GND	1PERp7	1PERn7	GND

Table B-4. XP4 Connector Pinout for the System Controller Slot

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	RSV	RSV	RSV	RSV	RSV	GND
4	GND	RSV	RSV	RSV	RSV	RSV	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	RSV	PXI_STAR	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	RSV	GND	PXI_TRIG7	GND
8	GND	RSV	GND	RSV	RSV	PXI_LBR6	GND

System Timing Slot Pinouts

Table B-5. TP1 Connector Pinout for the System Timing Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_DSTARA3+	PXIe_DSTARA3-	GND	PXIe_DSTARC7+	PXIe_DSTARC7-	GND	PXIe_DSTARC12+	PXIe_DSTARC12-	GND
2	PXIe_DSTARC4+	PXIe_DSTARC4-	GND	PXI_STAR12	PXI_STAR13	GND	PXIe_DSTARA12+	PXIe_DSTARA12-	GND
3	PXIe_DSTARB4+	PXIe_DSTARB4-	GND	PXIe_DSTARB16+	PXIe_DSTARA16-	GND	PXIe_DSTARB12+	PXIe_DSTARB12-	GND
4	PXIe_DSTARA4+	PXIe_DSTARA4-	GND	PXIe_DSTARB7+	PXIe_DSTARB7-	GND	PXIe_DSTARC13+	PXIe_DSTARC13-	GND
5	PXIe_DSTARC5+	PXIe_DSTARC5-	GND	PXI_STAR14	PXI_STAR15	GND	PXIe_DSTARA13+	PXIe_DSTARA13-	GND
6	PXIe_DSTARB5+	PXIe_DSTARB5-	GND	PXIe_DSTARB16+	PXIe_DSTARB16-	GND	PXIe_DSTARB13+	PXIe_DSTARB13-	GND
7	PXIe_DSTARA5+	PXIe_DSTARA5-	GND	PXIe_DSTARA7+	PXIe_DSTARA7-	GND	PXIe_DSTARC14+	PXIe_DSTARC14-	GND
8	PXIe_DSTARC6+	PXIe_DSTARC6-	GND	PXI_STAR16	RSV	GND	PXIe_DSTARA14+	PXIe_DSTARA14-	GND
9	PXIe_DSTARB6+	PXIe_DSTARB6-	GND	PXIe_DSTARC15+	PXIe_DSTARC15-	GND	PXIe_DSTARB14+	PXIe_DSTARB14-	GND
10	PXIe_DSTARA6+	PXIe_DSTARA6-	GND	PXIe_DSTARB15+	PXIe_DSTARB15-	GND	PXIe_DSTARA15+	PXIe_DSTARA15-	GND

Table B-6. TP2 Connector Pinout for the System Timing Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_DSTARC0+	PXIe_DSTARC0-	GND	PXIe_DSTARC8+	PXIe_DSTARC8-	GND	PXIe_DSTARB8+	PXIe_DSTARB8-	GND
2	PXIe_DSTARA0+	PXIe_DSTARA0-	GND	PXIe_DSTARC9+	PXIe_DSTARC9-	GND	PXIe_DSTARA8+	PXIe_DSTARA8-	GND
3	PXIe_DSTARB0+	PXIe_DSTARB0-	GND	PXIe_DSTARC1+	PXIe_DSTARC1-	GND	PXIe_DSTARA9+	PXIe_DSTARA9-	GND
4	PXIe_DSTARB1+	PXIe_DSTARB1-	GND	PXI_STAR0	PXI_STAR1	GND	PXIe_DSTARB9+	PXIe_DSTARB9-	GND
5	PXIe_DSTARA1+	PXIe_DSTARA1-	GND	PXI_STAR2	PXI_STAR3	GND	PXIe_DSTARC10+	PXIe_DSTARC10-	GND
6	PXIe_DSTARC2+	PXIe_DSTARC2-	GND	PXI_STAR4	PXI_STAR5	GND	PXIe_DSTARA10+	PXIe_DSTARA10-	GND
7	PXIe_DSTARB2+	PXIe_DSTARB2-	GND	PXI_STAR6	PXI_STAR7	GND	PXIe_DSTARB10+	PXIe_DSTARB10-	GND
8	PXIe_DSTARA2+	PXIe_DSTARA2-	GND	PXI_STAR8	PXI_STAR9	GND	PXIe_DSTARC11+	PXIe_DSTARC11-	GND
9	PXIe_DSTARC3+	PXIe_DSTARC3-	GND	PXI_STAR10	PXI_STAR11	GND	PXIe_DSTARA11+	PXIe_DSTARA11-	GND
10	PXIe_DSTARB3+	PXIe_DSTARB3-	GND	PXIe_DSTARC16+	PXIe_DSTARC16-	GND	PXIe_DSTARB11+	PXIe_DSTARB11-	GND

Table B-7. XP3 Connector Pinout for the System Timing Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_CLK100+	PXIe_CLK100-	GND	PXIe_SYNC100+	PXIe_SYNC100-	GND	PXIe_DSTARC+	PXIe_DSTARC-	GND
2	PRSNT#	PWREN#	GND	PXIe_DSTARB+	PXIe_DSTARB-	GND	PXIe_DSTARA+	PXIe_DSTARA-	GND
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND
4	MPWRGD*	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND

Table B-8. XP4 Connector Pinout for the System Timing Slot

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	ATNLED	PXI_CLK10_IN	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND
8	GND	PXIe_SYNC_CTRL	GND	RSV	PXI_LBL6	PXI_LBR6	GND

Peripheral Slot Pinouts

Table B-9. P1 Connector Pinout for the Peripheral Slot

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12 to 14	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY	V(I/O)	INTP	INTS	GND

Table B-9. P1 Connector Pinout for the Peripheral Slot (Continued)

Pin	Z	A	B	C	D	E	F
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

Table B-10. P2 Connector Pinout for the Peripheral Slot

Pin	Z	A	B	C	D	E	F
22	GND	**GA4**	**GA3**	**GA2**	**GA1**	**GA0**	GND
21	GND	**PXI_LBR0**	GND	**PXI_LBR1**	**PXI_LBR2**	**PXI_LBR3**	GND
20	GND	**PXI_LBR4**	**PXI_LBR5**	**PXI_LBL0**	GND	**PXI_LBL1**	GND
19	GND	**PXI_LBL2**	GND	**PXI_LBL3**	**PXI_LBL4**	**PXI_LBL5**	GND
18	GND	**PXI_TRIG3**	**PXI_TRIG4**	**PXI_TRIG5**	GND	**PXI_TRIG6**	GND
17	GND	**PXI_TRIG2**	GND	RSV	**PXI_STAR**	**PXI_CLK10**	GND
16	GND	**PXI_TRIG1**	**PXI_TRIG0**	RSV	GND	**PXI_TRIG7**	GND
15	GND	**PXI_BRSVA15**	GND	RSV	**PXI_LBL6**	**PXI_LBR6**	GND
14	GND	RSV	RSV	RSV	GND	RSV	GND
13	GND	RSV	GND	V(I/O)	RSV	RSV	GND
12	GND	RSV	RSV	RSV	GND	RSV	GND
11	GND	RSV	GND	V(I/O)	RSV	RSV	GND
10	GND	RSV	RSV	RSV	GND	RSV	GND
9	GND	RSV	GND	V(I/O)	RSV	RSV	GND
8	GND	RSV	RSV	RSV	GND	RSV	GND
7	GND	RSV	GND	V(I/O)	RSV	RSV	GND
6	GND	RSV	RSV	RSV	GND	RSV	GND
5	GND	RSV	GND	V(I/O)	RSV	RSV	GND
4	GND	V(I/O)	64EN#	RSV	GND	RSV	GND
3	GND	**PXI_LBR7**	GND	**PXI_LBR8**	**PXI_LBR9**	**PXI_LBR10**	GND
2	GND	**PXI_LBR11**	**PXI_LBR12**	UNC	**PXI_LBL7**	**PXI_LBL8**	GND
1	GND	**PXI_LBL9**	GND	**PXI_LBL10**	**PXI_LBL11**	**PXI_LBL12**	GND

Hybrid Slot Pinouts

Table B-11. P1 Connector Pinout for the Hybrid Slot

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12 to 14	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

Table B-12. XP3 Connector Pinout for the Hybrid Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXIe_CLK100+	PXIe_CLK100-	GND	PXIe_SYNC100+	PXIe_SYNC100-	GND	PXIe_DSTARC+	PXIe_DSTARC-	GND
2	PRSNT#	PWREN#	GND	PXIe_DSTARB+	PXIe_DSTARB-	GND	PXIe_DSTARA+	PXIe_DSTARA-	GND
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND
4	MPWRGD*	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND

Table B-13. XP4 Connector Pinout for the Hybrid Slot

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	ATNLED	PXI_STAR	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND
8	GND	RSV	GND	RSV	PXI_LBL6	PXI_LBR6	GND

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Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
µ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}
G	giga	10^{9}
T	tera	10^{12}

Symbols

°	Degrees.
≥	Equal or greater than.
≤	Equal or less than.
%	Percent.

A

A	Amperes.
AC	Alternating current.
ANSI	American National Standards Institute.
Auto	Automatic fan speed control.
AWG	American Wire Gauge.

B

backplane	An assembly, typically a printed circuit board, with connectors and signal paths that bus the connector pins.

C

C	Celsius.
cfm	Cubic feet per minute.
CFR	Code of Federal Regulations.
cm	Centimeters.
CompactPCI	An adaptation of the Peripheral Component Interconnect (PCI) Specification 2.1 or later for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI. It uses industry standard mechanical components and high-performance connector technologies to provide an optimized system intended for rugged applications. It is electrically compatible with the PCI Specification, which enables low-cost PCI components to be utilized in a mechanical form factor suited for rugged environments.
CSA	Canadian Standards Association.

D

daisy-chain	A method of propagating signals along a bus, in which the devices are prioritized on the basis of their position on the bus.
DC	Direct current.
DoC	Declaration of Conformity.

E

efficiency	Ratio of output power to input power, expressed as a percentage.
EIA	Electronic Industries Association.

EMC	Electromagnetic Compatibility.
EMI	Electromagnetic Interference.

F

FCC	Federal Communications Commission.
filler panel	A blank module front panel used to fill empty slots in the chassis.

G

g	(1) grams; (2) a measure of acceleration equal to 9.8 m/s^2.
GPIB	General Purpose Interface Bus (IEEE 488).
g_{RMS}	A measure of random vibration. The root mean square of acceleration levels in a random vibration test profile.

H

hr	Hours.
Hz	Hertz; cycles per second.

I

IEC	International Electrotechnical Commission; an organization that sets international electrical and electronics standards.
IEEE	Institute of Electrical and Electronics Engineers.
I_{MP}	Mainframe peak current.
in.	Inches.
inhibit	To turn off.

J

jitter	A measure of the small, rapid variations in clock transition times from their nominal regular intervals. Units: seconds RMS.

K

kg	Kilograms.
km	Kilometers.

L

lb	Pounds.
LED	Light emitting diode.
line regulation	The maximum steady-state percentage that a DC voltage output will change as a result of a specified change in input AC voltage (step change from 90 to 132 VAC or 180 to 264 VAC).
load regulation	The maximum steady-state percentage that a DC voltage output will change as a result of a step change from no-load to full-load output current.

M

m	Meters.
MHz	Megahertz. One million Hertz; one Hertz equals one cycle per second.
mi	Miles.
ms	Milliseconds.
MTBF	Mean time between failure.
MTTR	Mean time to repair.

N

NEMA	National Electrical Manufacturers Association.
NI	National Instruments.

P

power supply shuttle	A removable module that contains the chassis power supply.
PXI	PCI eXtensions for Instrumentation.
PXI_CLK10	10 MHz PXI system reference clock.

R

RH	Relative humidity.
RMS	Root mean square.

S

s	Seconds.
skew	Deviation in signal transmission times.
slot blocker	An assembly installed into an empty slot to improve the airflow in adjacent slots.
SMA	SubMiniature version A connector; a commonly used coaxial connector.
standby	The backplane is unpowered (off), but the chassis is still connected to AC power mains.
System controller	A module configured for installation in Slot 1of a PXI chassis. This device is unique in the PXI system in that it performs the system controller functions, including clock sourcing and arbitration for data transfers across the backplane. Installing such a device into any other slot can damage the device, the PXI backplane, or both.

system reference clock	A 10 MHz clock, also called PXI_CLK10, that is distributed to all peripheral slots in the chassis, as well as a BNC connector on the rear of chassis labeled *10 MHz REF OUT*. The system reference clock can be used for synchronization of multiple modules in a measurement or control system. The 10 MHz REF IN and OUT BNC connectors on the rear of the chassis can be used to synchronize multiple chassis to one reference clock. The PXI backplane specification defines implementation guidelines for PXI_CLK10.
System Timing slot	This slot is located at slot 4 and has dedicated trigger lines to other slots.

T

TTL	Transistor-transistor logic.

U

UL	Underwriter's Laboratories.

V

V	Volts.
VAC	Volts alternating current.
V_{pp}	Peak-to-peak voltage.

W

W	Watts.

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Heinrich-Lorenz-Str. 55 Tel.: +49/371/38388-0
09120 Chemnitz Fax: +49/371/38388-99
E-Mail: info@amc-systeme.de Web: www.amc-systeme.de

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